WHLE-LS1 Datasheet

Version 2.0

- NXP LS1 Series SoC
- DPAA/DPAA2
- PCI Express
- USB 3.0 host mode
- USB 2.0 device mode
- DDR4 Memory
- eMMC Storage
- 2 x 10Gbit/s SFP+
- 4 x 1Gbit/s RJ45
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## 2. Revision history

Table 2.1 Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Author</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Mar 08, 2022</td>
<td></td>
<td>Initial - Preliminary</td>
</tr>
<tr>
<td>1.1</td>
<td>May 12, 2022</td>
<td></td>
<td>Review and detailed update of all sections</td>
</tr>
</tbody>
</table>
3. Overview

The Conclusive Engineering Whale WHLE-LS1 is a series of high-performance Single Board Computers. They are powered by the NXP QoriQ® Layerscape® SoC series, available in variants optimized for efficiency (based on ARM® Cortex®-A53) or computation power (based on ARM® Cortex®-A72). The SoC range is capable of delivering an approximate performance from 15,000 to 45,000 CoreMark.

WHLE-LS1 offers features typically associated with SmartNICs thanks to Layerscape’s integrated Data Path Acceleration Architecture, fully leveraged in board design. It offers fine-grained control over its 6 Ethernet connectors (4xRJ45, 2xSFP+) and advanced traffic routing and processing capabilities.

WHLE-LS1 is capable of native, hardware-supported real time operation.
Fig. 3.2 WHLE-LS1 board TOP view

Fig. 3.3 WHLE-LS1 board BOTTOM view
4. Features of WHLE-LS1

- NXP QorIQ Layerscape LS10xx SoC:
  - ARM Cortex-A53 or Cortex-A72 cores
  - 2/4/8 core variants
  - Clock up to 1.8GHz
- SODIMM DDR4 slot
  - Supports up to 32GB of SODIMM DDR4 memory
  - ECC support
  - Up to 2.1GT/s
- Connectivity
  - 2 SFP+ interfaces supporting 10000Mbps Ethernet
  - 4 RJ45 interfaces supporting 10/100/1000Mbps Ethernet
- Expansion slots
  - 1 PCIe M.2 x1 Key-E slot
  - 1 PCIe M.2 x1 Key-M slot
  - 1 PCIe M.2 x2 Key-M slot
- Software support
  - Mainline Linux kernel support
  - FreeBSD 13 support (on request)
  - Support for Open Portable Trusted Execution Environment (OP-TEE)
  - Supported Bootloaders:
    - U-Boot
    - UEFI EDK2
    - ARM Trusted Firmware
5. Block Diagram
6. Main hardware components

This section summarizes the main hardware building blocks of the WHLE-LS1 series single board computer.

6.1. NXP LS1 Series SoC

- 780 FC-PBGA package, 23 mm x 23 mm
- SoC Available in the following configurations:
  - LS1026A: Dual ARM Cortex-A72 64-bit cores, 2MB L2 cache
  - LS1046A: Quad ARM Cortex-A72 64-bit cores, 2MB L2 cache
  - LS1048A: Quad ARM Cortex-A53 64-bit cores, 1MB L2 cache
  - LS1088A: Octal ARM Cortex-A53 64-bit cores, 2x 1MB L2 cache
- Networking subsystem
  - DPAA (LS1026A, LS1046A)
  - DPAA2 (LS1048A, LS1088A)
- PCI Express interface
  - 3 controllers total, 2 used for internal devices
  - 1 controller available, providing 4 PCIe lanes total for user-attached devices
- USB subsystem
  - USB 3.0 SuperSpeed host
  - USB 2.0 High Speed device
6.2. DDR4 Memory slot

- One SODIMM 260-pin DDR4 slot, attached to the SoC 32/64 bit memory controller.
- Memory controller supports ECC and interleaving
- Transfer speeds up to 2.1GT/s
- Supports SODIMM DDR4 module capacity up to 32GB
6.3. eMMC Storage

- Supports eMMC 4.51 JEDEC standard
- Available capacities:
  - 4GB
  - 16GB
  - 64GB
- RPMB (Replay Protected Memory Block) available for Trusted Execution Environment applications
6.4. QSPI NOR Flash

GigaDevice GD25LQ128EWIGR 128MB QSPI NOR Flash on the back side of the board. Provides additional fast memory to the LS1 SoC.

- Up to 120MHz read
- Up to 480Mbits/s data transfer
- Typical data retention of 20 years
- 100,000 write/erase cycles (minimum)
- Optimized for fast SoC cache fill

XiP is unsupported.
6.5. EEPROM

Microchip 24LC64-I/SN 64Kbit EEPROM (8 blocks of 8Kbit)

- Typical page-write cycle time: 2 ms
- Hardware write protection for entire memory
- 1,000,000 erase/write cycles
- Data retention exceeds 200 years
- Operation temperature range: -40°C to +85°C
Realtek RTL8211FS-CG 4 Ethernet Physical Layer Transceivers on the back side of the board. They control the 4 available Ethernet ports. RTL8211FS-CG provides:

- hardware support for high-precision clock synchronization (based on PTP of IEEE 1588 and 802.1AS).
- crossover detection
- auto-correction
- polarity correction
- adaptive equalization
- cross-talk cancellation
- echo cancellation
- timing recovery
- error correction
6.7. Reset Button

Reset button. Pulls down the reset pin on the MAX16004ATP+ voltage supervisor, causing a full power cycle of the board. Internally, this causes a power cycle on all power domains, with the exception of VDD_1V8_SHDN and VDD_3V3_SHDN domains which supply power to the board’s reset tree and status LEDs. It can be used to wake the SoC from a shutdown state.
6.8. Power Switch

Power Switch, slide-type. In ON position shorts a signal line that activates the power supply circuit, which begins supplying power to the board components. It’s internally identical to the Power Switch header pins.
6.9. Power switch header

2-pin 2.54mm header. Functionally identical to the main power switch. When shorted it overrides the power switch, keeping the board in ON state regardless of the power switch position.

The pins provide signal to the power supply IC. When shorted, the IC begins a power on sequence.
6.10. LED power supply voltage indicator

Green color LED indicating presence of 12V power supply to the board.

The LED lights up when there is voltage present on the VIN- pin of Texas Instruments INA220A power monitoring IC.
6.11. LED Board States

LED Group indicating board states:

- Power Fault (Red). Lights up when there's an issue on any of the board's power rails, with the exception of the board's main 12V power supply.
- Reset (Yellow). Lights up when the reset button is pressed, or when the SoC performs a soft reset of the board.
- Shutdown (Yellow). Lights up when the SoC is in the shutdown state. To wake from shutdown, perform a full power cycle, or press the reset button.

The LEDs are connected to the board's Power Up Sequencer.
6.12. DIP switch for power boot selection

4 position DIP switch for boot source selection (QSPI Flash or eMMC).

For DIP switch configuration please refer to the Boot process and provisioning section of this document.
6.13. TA_PROG_SFP header

2-pin 1.27mm header.

WARNING: Pins must not be shorted during normal board operation.

TA_PROG_SFP header is intended for use only during programming of Secure Boot of the WHLE-LS1.

Shorting this header delivers 1.8V to the TA_PROG_SFP pin on the LS1 SoC. This enables Secure Boot configuration via fuse burning on the LS1 SoC.
6.14. RESET_REQ_B header

2-pin 1.27mm header.

WARNING: During normal operation, this header should always be shorted.

Breaking this header disables the SoC’s whole board soft reset capability by completely disconnecting it from the board’s reset tree. This is typically used in board JTAG programming or debugging scenarios, for example when the board becomes stuck in a reset loop.
6.15. RTC Clock

Microchip MCP79412T-I/MNY RTC Clock with Calendar:

- Hours, minutes, seconds, day of week, day, month, year
- Leap year: 2399
- 12 and 24-hour modes
- Programmable Alarms
- Power fail logging timestamps battery/VCC switchover events.
- V CC minimum values: 1.2 μA at 3.3V
- V BAT minimum values: 925 nA at 3.0V
- Automatic Switchover to Battery Backup
- 64-Byte Battery-Backed SRAM
- 1 Kbit EEPROM Memory with software write-protect, 1 000 000 erase/write cycles and 64-Bit Protected EEPROM Area
- Temperature Range: -40°C to +85°C
One CR2032 battery slot on the back side of the board. It’s connected directly to the VBAT pin of the MCP79412T-I/MNY Real Time Clock. Battery’s only function is to supply power to the RTC, and it does not power any other components.
6.17. Fan controller

Microchip EMC2302-1-AIZL-TR fan controller and status monitor. It has 2 PWM-based fan drivers. On WHLE-LS1 it’s responsible for controlling both available fan connectors. The fan controller features:

- fan spin up control
- ramp rate control
- fan stall alert
- watchdog timer
- 1% accuracy from 500 to 16000 RPM

The fan controller is available on the board’s I2C bus, and fully user programmable. In the default WHLE-LS1 configuration, the fan controller:

- is not programmed
- has the watchdog function turned on, and is expecting I2C communication within 4 seconds of receiving power.
- if no communication over I2C happens, the controller turns on all installed fans to 100%, and turns on the LED Fan Fault.

The fan controller’s alert pin is connected to the LED Fan Fault, and to the board’s GPIO expander.
Red color LED indicating an issue with the board fan. Fan status output is read from the EMC2302-1-AIZL-TR fan controller alert pin, and LED lights up when the fan controller detects an issue with any of the fans that are under its control.
6.19. Power monitor

Texas Instruments INA220A power monitoring IC. Available on the I2C bus. It monitors shunt drop and power supply voltage, measures power draw in amperes, and can calculate resulting power draw. It operates in the -40°C to +125°C range, consuming a maximum of 1mA. Its powered by the 3.3V bus.
6.20. LED User-Programmable

Two bi-color green/red LEDs with a light guide. User-programmable, can be used to display status, error codes, etc.

They are connected to an NXP CA9633DP1,118 bi-color LED driver which is present as an addressable device on the system's I2C bus.
7. Configuration

7.1. SerDes lane assignments

WHLE-LS1 series offers two SerDes modules (SerDes1 and SerDes2), each having four lanes supporting up to 10.3125Gbit/s speeds.

Table 7.1 SerDes 1 Lanes

<table>
<thead>
<tr>
<th>Lane</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD1_0</td>
<td>SFP+ interface (10.3125 Gbit/s)</td>
</tr>
<tr>
<td>SD1_1</td>
<td>SFP+ interface (10.3135 Gbit/s)</td>
</tr>
<tr>
<td>SD1_2</td>
<td>SGMII interface (1.25 Gbit/s)</td>
</tr>
<tr>
<td>SD1_3</td>
<td>SGMII interface (1.25 Gbit/s)</td>
</tr>
</tbody>
</table>

Table 7.2 SerDes 2 Lanes

<table>
<thead>
<tr>
<th>Lane</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD2_0</td>
<td>PCIe x1 (Gen3) connected to a M.2 Key-E slot (2.5/5/8Gbit/s)</td>
</tr>
<tr>
<td>SD2_1</td>
<td>PCIe x1 (Gen3) connected to a M.2 Key-M slot (2.5/5/8Gbit/s)</td>
</tr>
<tr>
<td>SD2_2</td>
<td>PCIe x2 (Gen3) connected to a M.2 Key-E slot (2.5/5/8Gbit/s)</td>
</tr>
<tr>
<td>SD2_3</td>
<td>Complementary to PCIe on SD2_2</td>
</tr>
</tbody>
</table>
7.2. I2C peripherals

7.2.1. SYS_I2C (I2C1)

Table 7.3 SYS_I2C address table

<table>
<thead>
<tr>
<th>Address</th>
<th>Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x03</td>
<td>Led controller (soft reset)</td>
</tr>
<tr>
<td>0x18</td>
<td>XFI retimer</td>
</tr>
<tr>
<td>0x22</td>
<td>IO expander</td>
</tr>
<tr>
<td>0x2E</td>
<td>Fan controller</td>
</tr>
<tr>
<td>0x40</td>
<td>Power supply current monitor</td>
</tr>
<tr>
<td>0x50</td>
<td>SODIMM DDR4 slot</td>
</tr>
<tr>
<td>0x56</td>
<td>64kb EEPROM</td>
</tr>
<tr>
<td>0x57</td>
<td>1kb EEPROM (in RTC)</td>
</tr>
<tr>
<td>0x62</td>
<td>LED controller</td>
</tr>
<tr>
<td>0x6A</td>
<td>Clocks generator</td>
</tr>
<tr>
<td>0x6F</td>
<td>RTC</td>
</tr>
<tr>
<td>0x70</td>
<td>LED controller (all call)</td>
</tr>
</tbody>
</table>

7.2.2. AUX_I2C (I2C3)

Table 7.4 AUX_I2C address table

<table>
<thead>
<tr>
<th>Address</th>
<th>Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x70</td>
<td>I2C multiplexer</td>
</tr>
<tr>
<td>0x–</td>
<td>Channel 0</td>
</tr>
<tr>
<td></td>
<td>PCIe M.2 x1 Key-E slot</td>
</tr>
</tbody>
</table>
### 7.3. UART configuration

#### 7.3.1. DEBUG_UART (UART1)

Debug/console UART available on the microUSB connector via the FTDI FT230XQ-R USB to Basic Serial UART IC. It can be switched to expose the UART on the Conclusive Developer Cable connector instead. Switching is performed by the GPIO_3 pin on the Developer Cable connector.

#### 7.3.2. PCIE1_UART (UART2)

Connected to the M.2 Key-E PCIe connector.

<table>
<thead>
<tr>
<th>Address</th>
<th>Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x50/0x51</td>
<td>Channel 1</td>
</tr>
<tr>
<td>0x50/0x51</td>
<td>Channel 2</td>
</tr>
<tr>
<td>0x-</td>
<td>Channel 3</td>
</tr>
</tbody>
</table>
8. External connectors

8.1. Power connector

Default board power supply connector, a 12V DC, 2.5x6.5mm female power jack socket, symbol PJ-202BH. Expects a matching male connector with the external contact negative, and the internal contact positive.
8.2. Ethernet RJ-45 connectors

Four RJ45 connectors with LED status indicators. Each is capable of 10/100/1000 Mbit/s bandwidth, and each of the ports is controlled by a Realtek RTL8211FS-CG PHY oriented on the back side of the board.
8.3. SFP+ connectors

Two SFP+ connectors. Each is capable of 1000/10000 Mbit/s bandwidth. LED indicators are implemented via plastic light guides that overlay the SFP+ connector. They are transmitting light from SMD LEDs mounted directly on board. The LEDs are a part of the SFP+ circuit, and are not user-accessible.
8.4. LED SFP+ Indicators

SFP+ activity indicators LEDs covered with plastic light guides. They are directly wired to the SFP+ controller.
8.5. M.2 PCIe slots

M.2 PCIe slots:

- Key-E 1x PCIe slot (J3),
- Key-M 1x PCIe slot (J4),
- Key-M 2x PCIe slot (J5).

Key-E is intended for a wireless card or an expansion module, but apart from its dimensions it is functionally identical to Key-M slots. For storage purposes, the PCIe slots support NVMe SSDs. SATA SSDs are not supported. M.2 SATA controllers and other PCIe devices should be supported, but may require additional drivers or other modifications. In case of issues with M.2 devices, please contact us.
8.6. USB connectors

USB connectors:

- Two (LS10x6) or one (LS10x8) USB 3.0 Type-A ports (J8).
- One USB 2.0 Micro-B port for DEBUG_UART via FT230X (J7).
8.7. LED USB 3.0 Status

Green color LEDs. They indicate USB port activity.

WHLE-LS1 comes with one or two USB ports, depending on the SoC. When two ports are present, they are stacked vertically.

USB1 LED indicates activity on the lower port, that’s present regardless of WHLE-LS1 variant. USB3 LED indicates activity of the upper port, if present.
8.8. LED UART status

LED Group indicating UART status, used for UART over USB debugging:

- Vbus (Green). Turns on when the USB cable is properly connected to the debug serial port.
- RX (Yellow). Blinks on data transfer.
- TX (Yellow). Blinks on data transfer.

The LEDs are connected to FT230XQ-R, USB to Basic UART IC.
8.9. GPIO header

General purpose header. Contains power output, six GPIO lanes and an I2C interface.

Table 8.1 General purpose header pinout

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC_3V3</td>
<td>Power</td>
<td>3.3V provided by the board</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>3</td>
<td>GPIO0</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>4</td>
<td>GPIO1</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>5</td>
<td>GPIO2</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>6</td>
<td>GPIO3</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>7</td>
<td>GPIO4</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>8</td>
<td>GPIO5</td>
<td>In/Out</td>
<td>General purpose input-output, connected directly to CPU</td>
</tr>
<tr>
<td>9</td>
<td>SCL</td>
<td>Out</td>
<td>AUX_I2C clock via multiplexer channel 3, 3.3V</td>
</tr>
<tr>
<td>10</td>
<td>SDA</td>
<td>In/Out</td>
<td>AUX_I2C data via multiplexer channel 3, 3.3V</td>
</tr>
</tbody>
</table>
8.10. Fan connectors

- One 3-pin 2.54mm standard fan connector (P2).
- One 4-pin 2.54mm standard fan connector (P6).

Both are controlled via the Microchip EMC2302-1-AIZL-TR fan controller.
8.11. Developer cable connector

Conclusive Developer Cable connector. 20-pin 1.27mm pitch. Composite header providing access to the following peripherals:

- JTAG (with control signals)
- UART (DEBUG_UART)
- I2C (SYS_I2C)
- EEPROM write protection signal
- Board reset inputs

Pinout:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC_IO</td>
<td>Power</td>
<td>Reference I/O voltage provided by the board</td>
</tr>
<tr>
<td>2</td>
<td>JTAG_TMS</td>
<td>In</td>
<td>JTAG test mode select</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>4</td>
<td>JTAG_TCK</td>
<td>In</td>
<td>JTAG clock</td>
</tr>
<tr>
<td>5</td>
<td>UART_RXD</td>
<td>Out</td>
<td>DEBUG_UART data receive signal</td>
</tr>
<tr>
<td>6</td>
<td>JTAG_TDO</td>
<td>Out</td>
<td>JTAG data output</td>
</tr>
<tr>
<td>Pin</td>
<td>Pin name</td>
<td>Direction</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>----------------</td>
<td>-----------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>7</td>
<td>UART_TXD</td>
<td>In</td>
<td>DEBUG_UART data transmit signal</td>
</tr>
<tr>
<td>8</td>
<td>JTAG_TDI</td>
<td>In</td>
<td>JTAG data input</td>
</tr>
<tr>
<td>9</td>
<td>JTAG_nTRST</td>
<td>In</td>
<td>JTAG test reset (active low)</td>
</tr>
<tr>
<td>10</td>
<td>JTAG_nRESET</td>
<td>In</td>
<td>JTAG reset (active low)</td>
</tr>
<tr>
<td>11</td>
<td>I2C_SCL</td>
<td>In/Out</td>
<td>SYS_I2C clock</td>
</tr>
<tr>
<td>12</td>
<td>JTAG_BSR_VSEL</td>
<td>In</td>
<td>An IEEE 1149.1 JTAG Compliance Enable</td>
</tr>
<tr>
<td>13</td>
<td>I2C_SDA</td>
<td>In/Out</td>
<td>SYS_I2C data</td>
</tr>
<tr>
<td>14</td>
<td>JTAG_TBSCAN_EN</td>
<td>In</td>
<td>An IEEE 1149.1 JTAG Compliance Enable</td>
</tr>
<tr>
<td>15</td>
<td>EEPROM_WP</td>
<td>In</td>
<td>EEPROM write protection (active low)</td>
</tr>
<tr>
<td>16</td>
<td>DEBUG_UART_MUX</td>
<td>In</td>
<td>Switch DEBUG_UART between Developer cable connector and Micro-B USB port</td>
</tr>
<tr>
<td>17</td>
<td>JTAG_HRESET_B</td>
<td>In</td>
<td>HRESET input (active low)</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>Power</td>
<td>Ground</td>
</tr>
</tbody>
</table>
9. Electrical specifications

9.1. Absolute maximum ratings

Table 9.1 Absolute maximum ratings

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Max Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Platform Supply Voltage</td>
<td>15</td>
<td>V</td>
</tr>
</tbody>
</table>

9.2. Recommended operating conditions

Table 9.2 Recommended operating conditions

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Recommended Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Platform Supply Voltage</td>
<td>12</td>
<td>V</td>
</tr>
</tbody>
</table>

9.3. Power consumption

Average power consumption in idle state: 6-8 Watts.

Maximum power consumption: 72W

To gather real application power consumption statistics, please use the built-in Texas Instruments INA220A power monitoring IC available on the board’s I2C bus. It provides advanced power monitoring features.

9.4. Recommended power supply:

WHLE-LS1 typically comes with a matching power supply. In case a power supply is not available, please use a matching 12V power supply capable of delivering at least 6A, with a matching connector as described in the Power connector section.
10. Environmental Specifications

Table 10.1 Environmental specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature range</td>
<td>0°C</td>
<td>+85°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-60°C</td>
<td>+120°C</td>
</tr>
<tr>
<td>SoC Junction temperature</td>
<td>0°C</td>
<td>+85°C</td>
</tr>
</tbody>
</table>

WARNING: System with an installed CR2032 battery must not exceed the temperature range of 0°C to +30°C at any time due to battery temperature limits.

To exceed this limit, please remove or change the CR2032 battery to one certified for target temperature use.
11. Mechanical drawings
Front side

Back side

- Overall height with included heatsink and cooling fan: 34mm
9.4. Recommended power supply:
Front side

Back side

9.4. Recommended power supply:
9.4. Recommended power supply:
12. Boot process and provisioning

This chapter describes the possible boot options and the initial device provisioning process. WHLE-LS1 can boot from 3 possible sources:

- eMMC
- QSPI
- JTAG.

12.1. RCW configuration

RCW, the Reset Configuration Word, can be configured by the on-board DIP switch. The DIP switch numbers [1, 2, 3, 4], as marked in the table below, correspond to the bit order of the RCW [8, 6, 4, 2].

<table>
<thead>
<tr>
<th>CPU</th>
<th>RCW source</th>
<th>Dip switch positions [1,2,3,4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LS10x6A</td>
<td>eMMC</td>
<td>ON - ON - ON - ON</td>
</tr>
<tr>
<td>LS10x6A</td>
<td>QSPI</td>
<td>ON - OFF - ON - ON</td>
</tr>
<tr>
<td>LS10x8A</td>
<td>eMMC</td>
<td>ON - ON - ON - OFF</td>
</tr>
<tr>
<td>LS10x8A</td>
<td>QSPI</td>
<td>OFF - OFF - ON - ON</td>
</tr>
</tbody>
</table>
13. Ordering information

WHLE-LS1 comes in several variants, with different CPUs and eMMC sizes. The available options are:

### 13.1. CPU variant

**Table 13.1 Available CPU variants**

<table>
<thead>
<tr>
<th>Part number</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>WHLE-LS1026A</td>
<td>NXP LS1026A SoC, dual core ARM Cortex-A72, DPAA</td>
</tr>
<tr>
<td>WHLE-LS1046A</td>
<td>NXP LS1046A SoC, quad core ARM Cortex-A72, DPAA</td>
</tr>
<tr>
<td>WHLE-LS1048A</td>
<td>NXP LS1048A SoC, quad core ARM Cortex-A53, DPAA2</td>
</tr>
<tr>
<td>WHLE-LS1088A</td>
<td>NXP LS1088A SoC, octa core ARM Cortex-A53, DPAA2</td>
</tr>
</tbody>
</table>

### 13.2. eMMC memory size

Below are the available options for the integrated eMMC memory.

**Table 13.2 eMMC memory size variants**

<table>
<thead>
<tr>
<th>eMMC size</th>
</tr>
</thead>
<tbody>
<tr>
<td>4GB</td>
</tr>
<tr>
<td>8GB</td>
</tr>
<tr>
<td>16GB</td>
</tr>
<tr>
<td>32GB</td>
</tr>
<tr>
<td>64GB</td>
</tr>
</tbody>
</table>

### 13.3. Ordering

To place an order, please visit our website at [https://store.conclusive.pl](https://store.conclusive.pl) or contact us directly.