

RCHD-PF Datasheet

Version 2.0

- 667MHz RISC-V
 - 4 compute cores
 - 1 realtime supervisor core
- PolarFire FPGA up to 254K LUTs
- Tamper resistant
- LPDDR4 RAM memory
- GPIO and HSIO
- Up to 64 GB onboard eMMC
- WiFi and 1Gbit Ethernet PHY
- 256 Mbit NOR Flash for FPGA configuration
- 30% smaller than a credit card
- Libero® SoC PolarFire FPGA Toolset

Table of Contents:

- 1. List of tables
- 2. Revision history
- 3. Overview
- 4. Features of RCHD-PF
 - 4.1. RISC-V Microprocessor Subsystem Features
 - 4.2. FPGA Features
 - 4.3. Low-Power Features
 - 4.4. Reliability Features
 - 4.5. Security Features
 - 4.6. Software features
- 5. Block diagram
- 6. Main hardware components
 - 6.1. PolarFire SoC FPGA
 - 6.2. LPDDR4 RAM
 - 6.3. eMMC
 - 6.4. NOR Flash
 - 6.5. USB OTG PHY
 - 6.6. WiFi transceiver
 - 6.7. Ethernet PHY
 - 6.8. EEPROM
 - 6.9. Real-time clock
 - 6.10. Power supply section
- 7. External connectors
 - 7.1. Wi-Fi Antenna Connector
 - 7.2. Board-to-board Connectors
- 8. Electrical Specifications
 - 8.1. Absolute Maximum Ratings
 - 8.2. Recommended Operating Conditions
 - 8.3. Output Power Supplies
- 9. Environmental Specifications
- 10. SOM Dimensions
- 11. Boot process
 - 11.1. Intro
- 12. Ordering information

1. List of tables

SoM Board-to-Board Connector J1

SoM Board-to-Board Connector J2

SoM Board-to-Board Connector J3

SoM Board-to-Board Connector J4

Absolute maximum ratings

Recommended operating conditions

Output power supplies

Environmental Specifications

2. Revision history

Table 2.1 Revision History

| Revision | Date | Notes |
|-----------------|--------------|--|
| 1 | Jan 04, 2020 | Initial - Preliminary |
| 2 | Apr 26, 2022 | Review and detailed update of all sections |

3. Overview

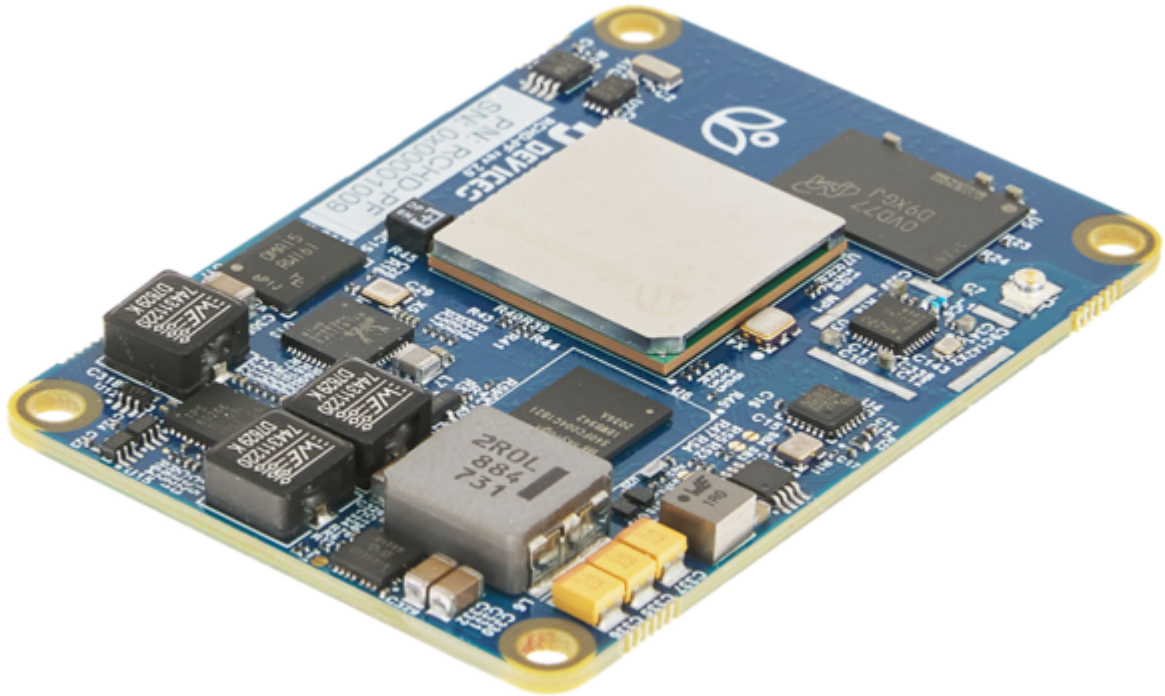


Fig. 3.1 RCHD-PF SOM module.

The Conclusive Engineering “Orchid” series RCHD-PF is a highly scalable System on Module. It carries a Microchip® PolarFire® System on Chip that contains a RISC-V CPU and an FPGA.

Orchid supports the full lineup of PolarFire® SoCs that use the FCVG 484 package. The RISC-V is a deterministic, coherent CPU cluster, composed of 5 cores - 4 general purpose cores, and a single supervisor core. It remains the same across the whole PolarFire® lineup, at around 2030 CoreMark performance at 667MHz. The FPGA can scale from 23K to 254K LUTs. The FPGA and the CPU use a shared, deterministic L2 memory subsystem.

Orchid is extremely power efficient. Its SoC is capable of delivering 6500 CoreMarks at 1.3W, and is up to 55% more efficient than closest comparable non-RISC-V solutions. It supports deterministic, asymmetric, hard real-time processing with memory coherence across the RISC-V cores and the FPGA. These applications can run either on bare metal, or alongside an operating system like Linux or FreeBSD. It is capable of dual 4K video processing.

Orchid is extremely secure. It can work in environments physically accessible by adversaries. It's secured against non-invasive data extraction by Differential Power Analysis, a patented

technology of Cryptography Research Incorporated. Its processor is fingerprinted using PUF, a Physically Unclonable Function. It changes its output on any tampering attempt that modifies the processor state.

Orchid's RISC-V CPU is a simple, 5-stage single issue in-order pipeline processor. It's resistant against Meltdown and Spectre types of exploits that are hard to mitigate on out-of-order CPUs.

Orchid's mainboard is 30% smaller than a credit card. It's typically delivered with a much larger evaluation daughterboard, the RCHD-PF-EVAL, which is also purchasable separately, and provides a breakout of Orchid's most important functionality to standardized connectors. We can provide custom daughterboards made to client's requirements, or customize Orchid itself.

Orchid's intended applications are:

- Imaging, Machine Vision, Smart Cameras (software & hardware control)
- Digital Signal Processing
- Endpoint Artificial Intelligence/Machine Learning (AI/ML)
- Internet of Things (IoT)
- Industrial Automation, Smart Factory, Advanced Sensor Fusion
- Automotive
- Aerospace and Defense
- Wireline Access Networks
- Cellular Infrastructure
- Virtual networks (software-programmable network infrastructure)

To learn more about the PolarFire SoC, please visit the [PolarFire SoC FPGA official page](#).

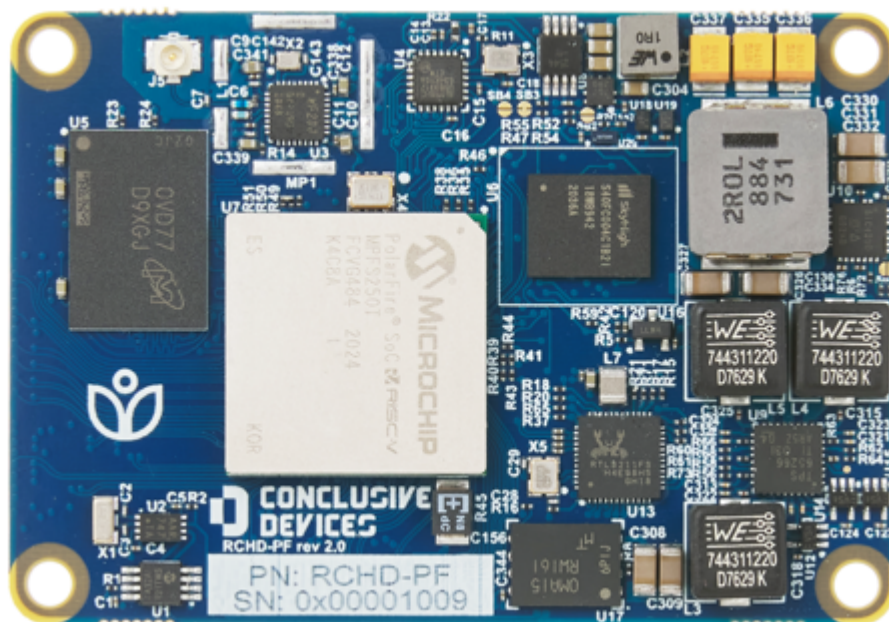


Fig. 3.2 RCHD-PF SOM module TOP view.

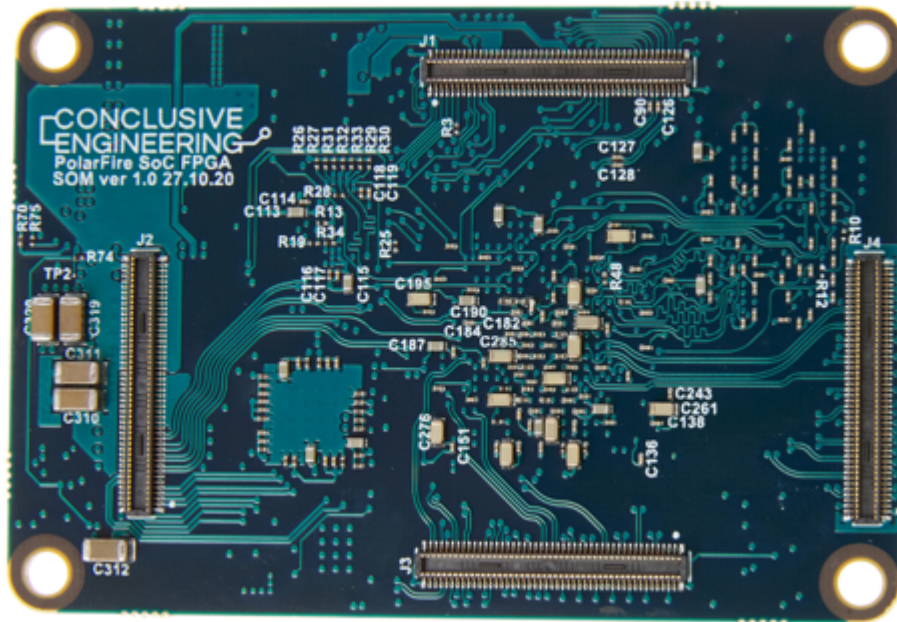


Fig. 3.3 RCHD-PF SOM module BOTTOM view.

4. Features of RCHD-PF

4.1. RISC-V Microprocessor Subsystem Features

- 4x 64-bit RV64GC Application processing core:
 - Fmax of 667 MHz (-40 °C to 100 °C Tj),
 - Benchmark performance: 3.0 CoreMarks®/MHz, 2.0 DMIPs/MHz:
 - L1 memory subsystem with single-error correct, double-error detect (SECEDED)
 - 32 Kbytes 8-way instruction cache or optional 28 Kbytes tightly integrated memory
 - 32 Kbytes 8-way data cache
 - Memory Management Unit (MMU)
 - Physical Memory Protection (PMP) unit
- 1x 64-bit RV64IMAC monitor processor core: - Fmax of 667 MHz (-40 °C to 100 °C Tj), 3.0 CoreMarks®/MHz, 2.0 DMIPs/MHz - L1 memory subsystem with SECEDED - 16 Kbytes 2-way instruction cache - 8 Kbytes scratch pad memory - PMP unit
- Flexible 2 MB L2 memory subsystem with SECEDED configurable as:
 - 16-way set associative L2 cache
 - Loosely Integrated Memory (LIM) mode for deterministic access
 - Coherent Scratchpad Memory mode for shared messages across cores
- Integrated 36-bit DDR4/DDR3/LPDDR4/LPDDR3 memory controller with SECEDED
 - DDR4 at 1.6 Gbps with a 8 GB address reach
 - RCHD-PF implements up to 4 GB LPDDR4 in a single die, soldered on board, but custom variants are possible
- Cache coherent CPU bus matrix
- AMBA I/O switch with QoS and memory protection

- Integrated 128 Kbytes embedded non-volatile memory (eNVM) for boot
- Boot options
 - Microchip secure boot
 - User defined, PUF-protected secure boot
 - Boot directly from eNVM
 - Platform interrupt controller
 - 185 interrupt sources from the microprocessor subsystem and FPGA fabric with seven priority levels

- Local interrupt controller
 - 48 local interrupts sourced from the FPGA drive the local interrupt controller on each core

- Debug
 - Ten hardware triggers per CPU (triggers can be configured as a breakpoint or a watchpoint)
 - Instruction trace on all CPUs
 - Performance counters
 - Runtime-configurable AXI bus monitors
 - Monitor AXI commands to DDR
 - Monitor an AXI port going into or out of the AMBA I/O AXI switch
 - 32-bit fabric monitor
 - SmartDebug
 - Dynamically monitor any two nets in the FPGA on two pins without changing the FPGA design
 - Read/write to FPGA flip-flops and memories
 - Halt clock trees, inspect logic tree
 - FPGA breakpoints
 - SmartDebug integrated into processor debug transport layer — debug from a single tool chain
 - Secure debug remotely over Ethernet (both the processor subsystem and the FPGA design)

- Processor I/O:
 - Two GigE MACs,
 - An USB 2.0 OTG,
 - MMC 5.1 SD/SDIO,
 - Two CAN 2.0, A and B,
 - Execute in place Quad SPI flash controller,
 - Five multi-mode UARTs,
 - Two SPI, two I2C,
 - RTC, GPIO,
 - Five watchdog timers,
 - Timers.

- Processor to FPGA Interconnect
 - Two 64-bit AXI4 processor-to-fabric interfaces
 - Three 64-bit AXI4 fabric-to-processor interfaces
 - A 32-bit APB processor-to-fabric interface

4.2. FPGA Features

- Up to 254K logic elements consisting of a 4-input look-up table (LUT) with a fracturable D-type flip-flop
- 20 Kbytes dual- or two-port large static random access memory (LSRAM) block with built-in SECEDED
- 64 × 12 two-port μ RAM block implemented as an array of latches
- 18 × 18 math block with a pre-adder, a 48-bit accumulator, and an optional 16-deep × 18 coefficient ROM
- Built-in μ PROM, modifiable at program time and readable at run time for user data storage
- High-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 12.7 Gbps
- Integrated dual x4 PCIe Gen2 endpoint (EP) and root port (RP) designs
- High-speed I/O (HSIO) supporting up to 1600 Mbps DDR4, 1333 Mbps DDR3L, and 1333 Mbps LPDDR3/DDR3 memories with integrated I/O digital
- General-purpose I/O (GPIO) supporting 3.3 V, built-in CDR for serial gigabit Ethernet, 1067 Mbps DDR3, and 1250 Mbps LVDS I/O speed with integrated I/O digital logic
- Low-power, phase-locked loops (PLLs) and delay-locked loops (DLLs) for high precision and low jitter
- 1.0 V and 1.05 V operating modes

4.3. Low-Power Features

- Low device static power
- Low inrush current
- Low-power transceivers

4.4. Reliability Features

- FPGA configuration cells single-event upset (SEU) immune
- Built-in SECEDED and memory interleaving on FPGA fabric LSRAMs

- SECDDED on all processor memories
- Error signals trapped and exported to the FPGA fabric
- System controller suspend mode for safety-critical designs

4.5. Security Features

- Cryptography Research Incorporated (CRI)-patented differential power analysis (DPA) bitstream protection
- Integrated dual physically unclonable function (PUF)
- 56 Kbytes of secure, non-volatile memory (sNVM)
- Built-in tamper detectors and countermeasures
- Digest integrity check for FPGA, μ PROM, sNVM, and eNVM

4.6. Software features

RCHD-PF is supported by the following software development environments:

- SoftConsole Embedded IDE
 - Eclipse IDE
 - Firmware catalog for device drivers

- Antmicro Renode™
 - Open Source PolarFire SoC System Modeling environment integrated with SoftConsole

- Libero® SoC PolarFire FPGA Toolset
 - Complete FPGA development environment
 - Includes Synplify Pro synthesis and Mentor ModelSim ME simulation

5. Block diagram

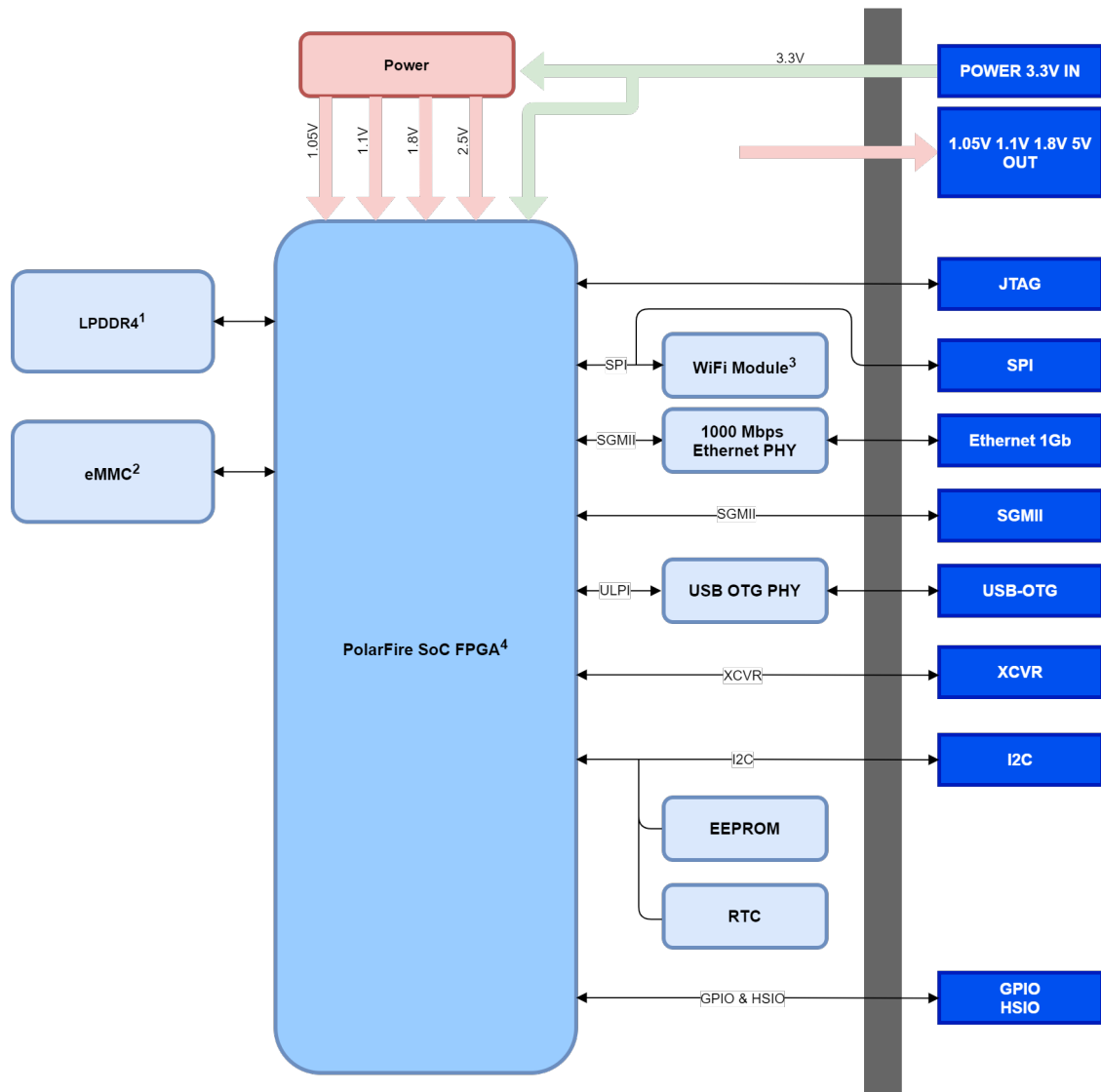


Fig. 5.1 Conclusive Engineering RCHD-PF SoM block diagram.

[1] Size and variant (LPDDR4) of RAM memory is determined by the SOM version.

[2] Size of EMMC memory is determined by the SOM version.

[3] WiFi module can be present or absent, determined by the SOM version. If absent, the MSS SPI interface is available on the header.

[4] Part number of PolarFire SoC FPGA is determined by the SOM version.

6. Main hardware components

This section summarizes the main hardware building blocks of the RCHD-PF.

6.1. PolarFire SoC FPGA

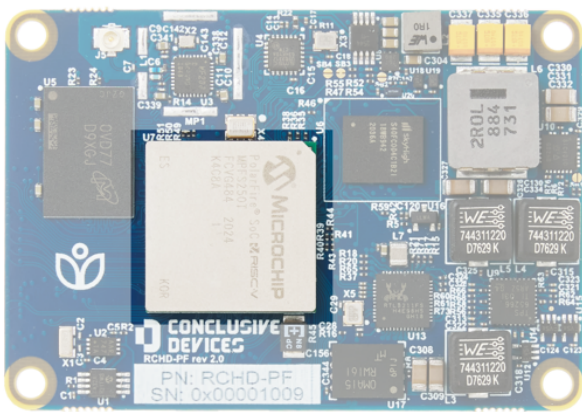


Fig. 6.1 PolarFire SoC on RCHD-PF.

For full specification of the PolarFire SoC please refer to subsection RISC-V Microprocessor Subsystem Features

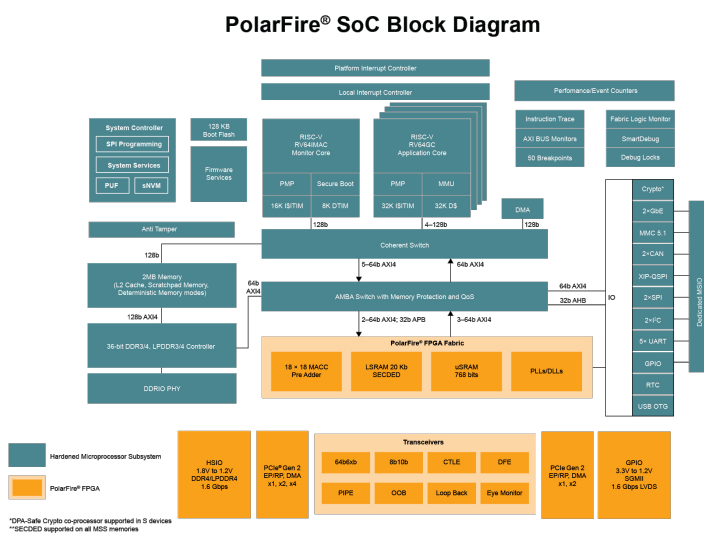


Fig. 6.2 PolarFire SoC block diagram.

6.2. LPDDR4 RAM

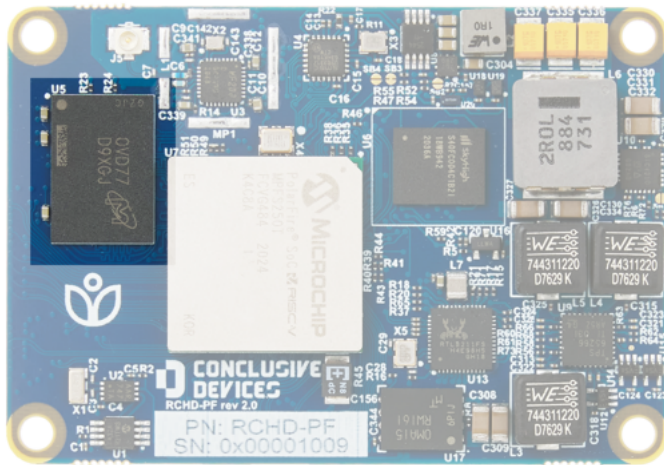


Fig. 6.3 RAM memory on RCHD-PF

The RCHD-PF is available with up to 4 GB of LPDDR4 memory operating at speeds up to 1600MTS.

6.3. eMMC

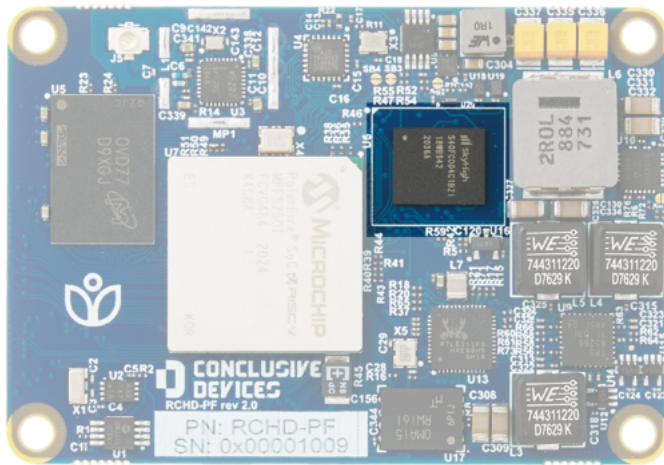


Fig. 6.4 eMMC on RCHD-PF.

RCHD-PF built-in eMMC memory, soldered directly on module. It is used for Flash Disk purposes, storage of Operating System run-time image, Boot-loader and application/user data storage. RCHD-PF can be ordered with different capacities of eMMC memory:

- 4 GB
- 16 GB
- 64 GB

6.4. NOR Flash

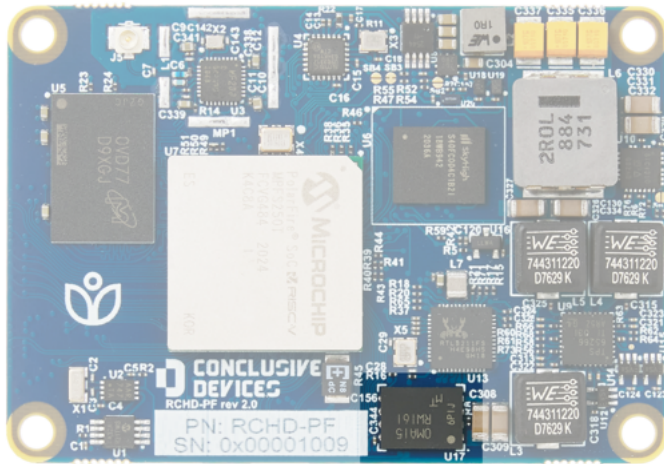


Fig. 6.5 NOR Flash on RCHD-PF

256 Mbit NOR Flash Memory for FPGA configuration.

6.5. USB OTG PHY

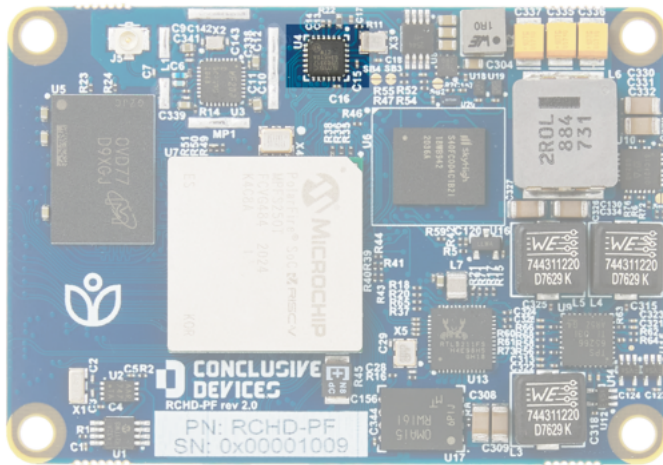


Fig. 6.6 USB OTG PHY on RCHD-PF

USB PHY based on USB3320 chip, a highly integrated full featured Hi-Speed USB 2.0 transceiver that utilizes Microchip's ULPI interface.

6.6. WiFi transceiver

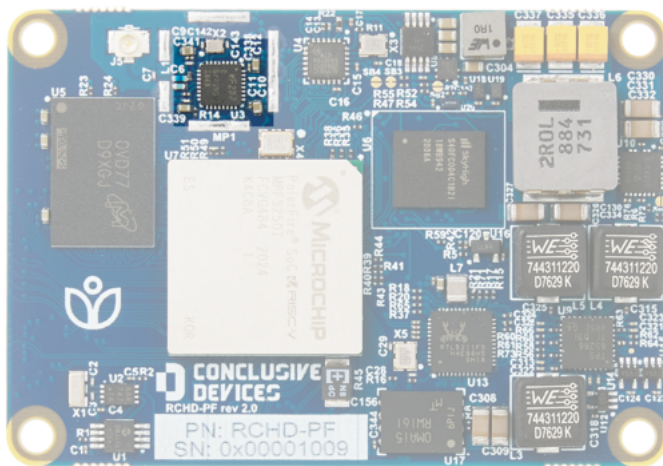


Fig. 6.7 WiFi transceiver on RCHD-PF

An ultra low power Wi-Fi WF200 chip from Silicon Labs. It's connected to the PolarFire SoC FPGA via an MSS SPI1 interface.

Key features:

- IEEE 802.11 b/g/n compliant
- TX power: +17 dBm (at pin)
- RX sensitivity: -96.7 dBm (at pin)
- Integrated antenna diversity support
- Ultra low power consumption
- Secure and signed software
- Encrypted host interface communication

6.7. Ethernet PHY

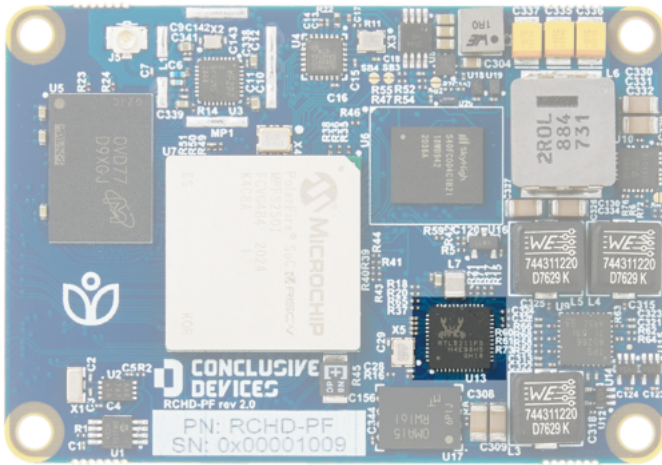


Fig. 6.8 Ethernet PHY on RCHD-PF

Low power 1Gbit ethernet transceiver based on Realtek RTL8211FS-CG PHY. It's connected to the PolarFire SoC FPGA via an SGMII interfaces.

6.8. EEPROM

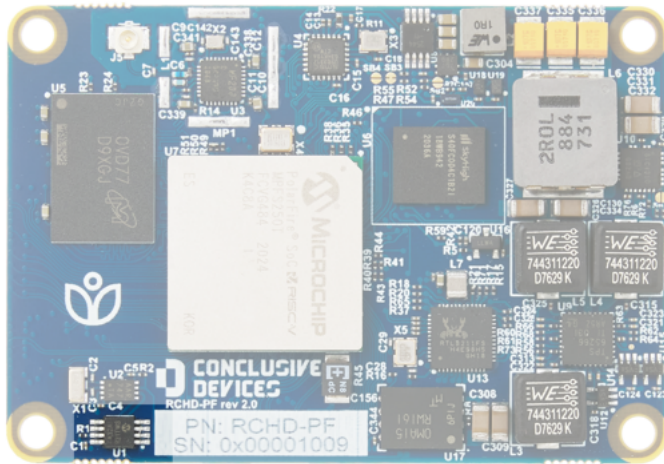


Fig. 6.9 EEPROM on RCHD-PF

A single 24AA32A EEPROM chip. EEPROM is accessible over I2C, with address 0x50. Its with Write Protect pin is available on the board-to-board connector J1. For exact pinouts, please refer to the External connectors section.

6.9. Real-time clock

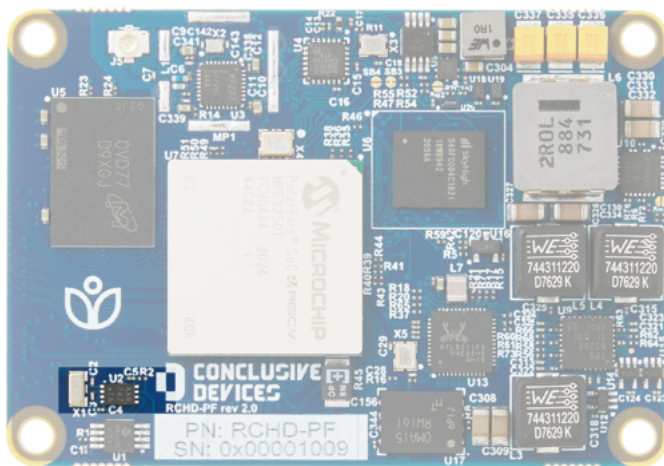


Fig. 6.10 RTC on RCHD-PF

A single MCP79412T RTC chip. RTC is accessible over I2C, with address 0x6F. Its VBAT power supply pin is available on the J3 connector. The VBAT pin is used only to supply power to the RTC. Its MFP

open-drain and alarm clockout pin is available on the J1 connector. For exact pinouts, please refer to the External connectors section.

6.10. Power supply section

RCHD-PF SoM has an extensive power supply section. Providing 3.3V to the SoM allows it to deliver voltages from 1.05V to 5V to the rest of the devices attached to it via the board-to-board connectors.

For more details, please refer to section [Output Power Supplies](#).

7. External connectors

With the exception of the antenna connector, all RCHD-PF board connectivity happens through the 4 board-to-board connectors on the back of the SoM.

To break out the board connectivity into standardized connectors, please use the RCHD-PF-EVAL evaluation module, or connect directly to the pins on the reverse of the board using a compatible connector, as described in the board-to-board connector section below.

7.1. Wi-Fi Antenna Connector

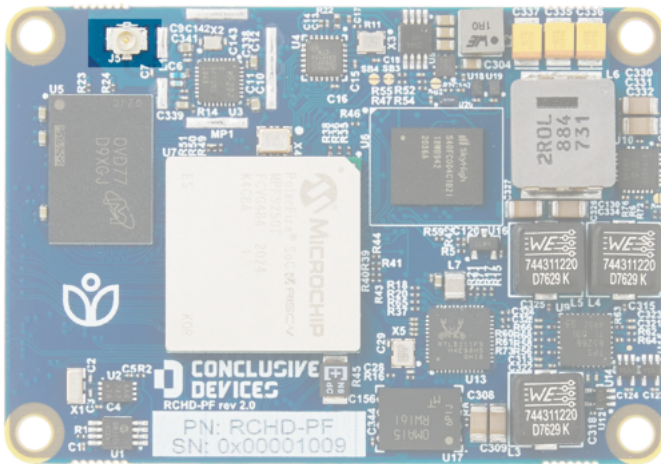


Fig. 7.1 Coaxial Wi-Fi connector

Orchid comes in variants with, or without the Wi-Fi module. Variants with the Wi-Fi module contain:

- One on-board U.FL Jack connector
- One compatible U.FL Jack connector antenna

To use a different antenna, please make sure it has a 50 Ohm characteristic impedance

7.2. Board-to-board Connectors

- The RCHD-PF exposes four 90-pin board-to-board connectors.
- The recommended mating connector is Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51).

7.2.1. Connector Numbering

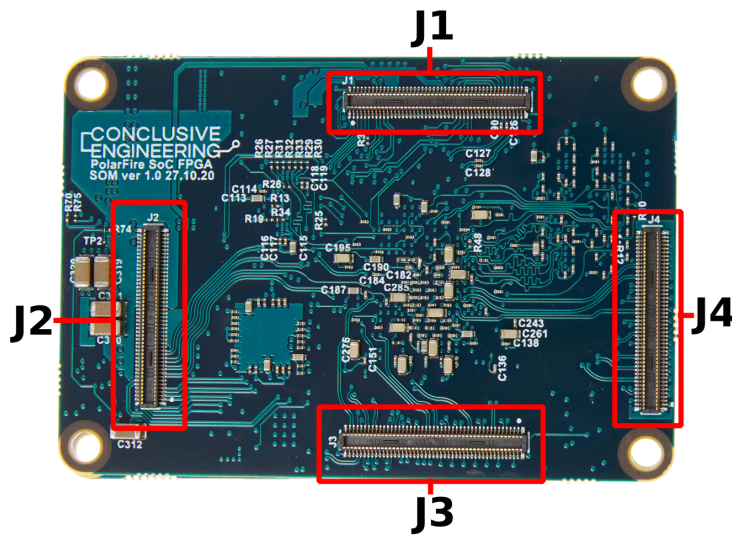


Fig. 7.2 Connector numbering on RCHD-PF (bottom view).

7.2.2. Connector J1 overview and pinouts

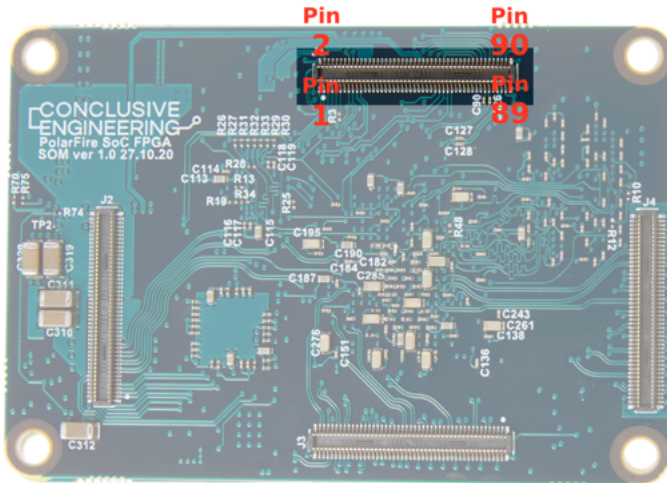


Fig. 7.3 Connector J1 on RCHD-PF (bottom view).

Connector J1 exposes the following connectivity of the RCHD-PF:

- Power supply pins
- JTAG
- USB
- I2C
- RTC
- MDIO
- UART
- Wifi RQ
- SPI

Table 7.1 SoM Board-to-Board Connector J1

| PIN # | Pin name | Description | Ball |
|-------|------------|-------------|------|
| J1_1 | JTAG_TRSTB | Input | G8 |
| J1_2 | VBUS | Input | |
| J1_3 | JTAG_TMS | Input | F8 |
| J1_4 | USB_ID | Input | |
| J1_5 | JTAG_TDO | Output | E8 |

| PIN # | Pin name | Description | Ball |
|--------------|----------------------|---------------------|-------------|
| J1_6 | USB_D_P | I/O | |
| J1_7 | JTAG_TDI | Input | G9 |
| J1_8 | USB_D_N | I/O | |
| J1_9 | JTAG_TCK | Input | E9 |
| J1_10 | EEPROM_WP | Input | |
| J1_11 | DEVRST_N | Input | H7 |
| J1_12 | RTC_MFP | Output | |
| J1_13 | MD_MDC | Output | D3 |
| J1_14 | SYS_I2C_SDA | I/O | B1 |
| J1_15 | MD_MDIO | I/O | C2 |
| J1_16 | SYS_I2C_SCL | Output | C1 |
| J1_17 | GPIO_1_22(UART0_TXD) | Output | E3 |
| J1_18 | VDD_5V | Power supply output | |
| J1_19 | GPIO_1_21(UART0_RXD) | Input | A3 |
| J1_20 | VDD_5V | Power supply output | |
| J1_21 | GND | Ground | |
| J1_22 | VDD_5V | Power supply output | |
| J1_23 | GND | Ground | |
| J1_24 | VDD_5V | Power supply output | |
| J1_25 | GND | Ground | |
| J1_26 | VDD_5V | Power supply output | |
| J1_27 | GND | Ground | |
| J1_28 | VDD_1V05 | Power supply output | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|---------------------|-------------|
| J1_29 | GND | Ground | |
| J1_30 | VDD_1V05 | Power supply output | |
| J1_31 | GND | Ground | |
| J1_32 | VDD_1V05 | Power supply output | |
| J1_33 | GND | Ground | |
| J1_34 | VDD_1V05 | Power supply output | |
| J1_35 | GND | Ground | |
| J1_36 | VDD_1V05 | Power supply output | |
| J1_37 | GND | Ground | |
| J1_38 | VDD_1V8 | Power supply output | |
| J1_39 | GND | Ground | |
| J1_40 | VDD_1V8 | Power supply output | |
| J1_41 | GND | Ground | |
| J1_42 | VDD_1V8 | Power supply output | |
| J1_43 | GND | Ground | |
| J1_44 | VDD_1V8 | Power supply output | |
| J1_45 | GND | Ground | |
| J1_46 | VDD_1V8 | Power supply output | |
| J1_47 | GND | Passive | |
| J1_48 | VDD_2V5 | Ground | |
| J1_49 | GND | Ground | |
| J1_50 | VDD_2V5 | Power supply output | |
| J1_51 | GND | Ground | |

| PIN # | Pin name | Description | Ball |
|--------------|---------------------|---------------------|-------------|
| J1_52 | VDD_2V5 | Power supply output | |
| J1_53 | GND | Ground | |
| J1_54 | VDD_2V5 | Power supply output | |
| J1_55 | GPIO_1_17(SPI_SS) | Output | E4 |
| J1_56 | VDD_2V5 | Power supply output | |
| J1_57 | GPIO_1_20(WIFI_IRQ) | Input | B3 |
| J1_58 | VDD_1V1 | Power supply output | |
| J1_59 | GPIO_1_19(SPI_SI) | Input | A2 |
| J1_60 | VDD_1V1 | Power supply output | |
| J1_61 | GPIO_1_18(SPI_DO) | Output | B2 |
| J1_62 | VDD_1V1 | Power supply output | |
| J1_63 | GPIO_1_16(SPI_SCK) | Output | E5 |
| J1_64 | VDD_1V1 | Power supply output | |
| J1_65 | GND | Ground | |
| J1_66 | VDD_1V1 | Power supply output | |
| J1_67 | GND | Ground | |
| J1_68 | GND | Ground | |
| J1_69 | GND | Ground | |
| J1_70 | GND | Ground | |
| J1_71 | GND | Ground | |
| J1_72 | GND | Ground | |
| J1_73 | GND | Ground | |
| J1_74 | GPIO169_P | I/O | C4 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J1_75 | GND | Ground | |
| J1_76 | GPIO169_N | I/O | B4 |
| J1_77 | GND | Ground | |
| J1_78 | GPIO170_P | I/O | C5 |
| J1_79 | SGMII_1_RX_P | Input | K6 |
| J1_80 | GPIO170_N | I/O | B5 |
| J1_81 | SGMII_1_RX_N | Input | K7 |
| J1_82 | GPIO172_P | I/O | A6 |
| J1_83 | GND | Ground | |
| J1_84 | GPIO172_N | I/O | A5 |
| J1_85 | SGMII_1_TX_P | Output | M7 |
| J1_86 | GPIO173_P | I/O | A7 |
| J1_87 | SGMII_1_TX_N | Output | N8 |
| J1_88 | GPIO173_N | I/O | B7 |
| J1_89 | GND | Ground | |
| J1_90 | GND | Ground | |

7.2.3. Connector J2 overview and pinouts

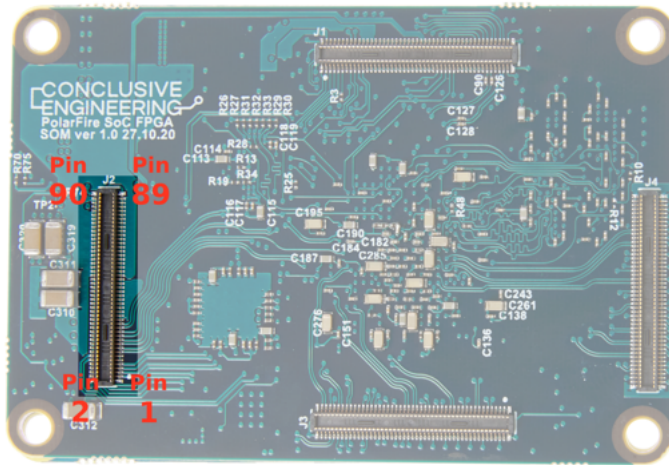


Fig. 7.4 Connector J2 on RCHD-PF (bottom view).

Connector J2 exposes the following connectivity of the RCHD-PF:

- Ethernet
- Power supply inputs
- General Purpose IO (GPIO)

Table 7.2 SoM Board-to-Board Connector J2

| PIN # | Pin name | Description | Ball |
|-------|------------|-------------|------|
| J2_1 | MDI_TRD3_P | I/O | |
| J2_2 | MDI_TRD1_P | I/O | |
| J2_3 | MDI_TRD3_N | I/O | |
| J2_4 | MDI_TRD1_N | I/O | |
| J2_5 | MDI_TRD4_P | I/O | |
| J2_6 | MDI_TRD2_P | I/O | |
| J2_7 | MDI_TRD4_N | I/O | |
| J2_8 | MDI_TRD2_N | I/O | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J2_9 | GND | Ground | |
| J2_10 | ETH_PHY_LED2 | I/O | |
| J2_11 | GND | Ground | |
| J2_12 | ETH_PHY_LED1 | I/O | |
| J2_13 | GPIO_183_P | I/O | D12 |
| J2_14 | GND | Ground | |
| J2_15 | GPIO_183_N | I/O | E11 |
| J2_16 | GND | Ground | |
| J2_17 | GPIO_0_P | I/O | B12 |
| J2_18 | GND | Ground | |
| J2_19 | GPIO_0_N | I/O | C12 |
| J2_20 | GND | Ground | |
| J2_21 | GPIO_177_P | I/O | A10 |
| J2_22 | GND | Ground | |
| J2_23 | GPIO_177_N | I/O | A11 |
| J2_24 | GND | Ground | |
| J2_25 | GPIO_176_P | I/O | C10 |
| J2_26 | GND | Ground | |
| J2_27 | GPIO_176_N | I/O | C9 |
| J2_28 | GND | Ground | |
| J2_29 | GND | Ground | |
| J2_30 | GND | Ground | |
| J2_31 | GND | Ground | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J2_32 | GND | Ground | |
| J2_33 | GND | Ground | |
| J2_34 | GND | Ground | |
| J2_35 | GND | Ground | |
| J2_36 | GND | Ground | |
| J2_37 | GND | Ground | |
| J2_38 | GND | Ground | |
| J2_39 | GND | Ground | |
| J2_40 | GND | Ground | |
| J2_41 | GND | Ground | |
| J2_42 | GND | Ground | |
| J2_43 | GND | Ground | |
| J2_44 | GND | Ground | |
| J2_45 | GND | Ground | |
| J2_46 | GND | Ground | |
| J2_47 | GND | Ground | |
| J2_48 | GND | Ground | |
| J2_49 | GND | Ground | |
| J2_50 | GND | Ground | |
| J2_51 | 3V3 | Power supply input | |
| J2_52 | 3V3 | Power supply input | |
| J2_53 | 3V3 | Power supply input | |
| J2_54 | 3V3 | Power supply input | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J2_55 | 3V3 | Power supply input | |
| J2_56 | 3V3 | Power supply input | |
| J2_57 | 3V3 | Power supply input | |
| J2_58 | 3V3 | Power supply input | |
| J2_59 | 3V3 | Power supply input | |
| J2_60 | 3V3 | Power supply input | |
| J2_61 | 3V3 | Power supply input | |
| J2_62 | 3V3 | Power supply input | |
| J2_63 | 3V3 | Power supply input | |
| J2_64 | 3V3 | Power supply input | |
| J2_65 | 3V3 | Power supply input | |
| J2_66 | 3V3 | Power supply input | |
| J2_67 | 3V3 | Power supply input | |
| J2_68 | 3V3 | Power supply input | |
| J2_69 | 3V3 | Power supply input | |
| J2_70 | 3V3 | Power supply input | |
| J2_71 | 3V3 | Power supply input | |
| J2_72 | 3V3 | Power supply input | |
| J2_73 | 3V3 | Power supply input | |
| J2_74 | 3V3 | Power supply input | |
| J2_75 | 3V3 | Power supply input | |
| J2_76 | 3V3 | Power supply input | |
| J2_77 | 3V3 | Power supply input | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J2_78 | 3V3 | Power supply input | |
| J2_79 | 3V3 | Power supply input | |
| J2_80 | 3V3 | Power supply input | |
| J2_81 | 3V3 | Power supply input | |
| J2_82 | 3V3 | Power supply input | |
| J2_83 | 3V3 | Power supply input | |
| J2_84 | 3V3 | Power supply input | |
| J2_85 | 3V3 | Power supply input | |
| J2_86 | 3V3 | Power supply input | |
| J2_87 | 3V3 | Power supply input | |
| J2_88 | 3V3 | Power supply input | |
| J2_89 | 3V3 | Power supply input | |
| J2_90 | 3V3 | Power supply input | |

7.2.4. Connector J3 overview and pinouts

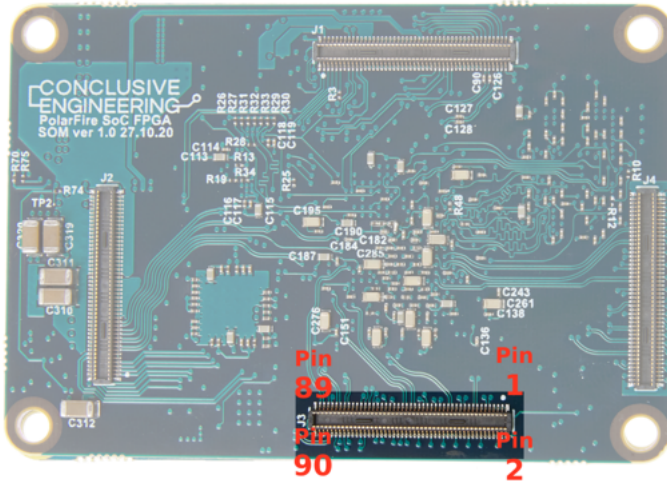


Fig. 7.5 Connector J3 on RCHD-PF (bottom view).

Connector J3 exposes the following connectivity of the RCHD-PF:

- Power supply inputs
- 4 x XCVR Bidirectional lanes (12.3 Gbit/s)
- General Purpose Input Output (GPIO)

Table 7.3 SoM Board-to-Board Connector J3

| PIN # | Pin name | Description | Ball |
|-------|--------------|--------------------|------|
| J3_1 | GND | Ground | |
| J3_2 | VBAT | Power supply input | |
| J3_3 | GND | Ground | |
| J3_4 | GND | Ground | |
| J3_5 | GND | Ground | |
| J3_6 | GND | Ground | |
| J3_7 | XCVR_0_TX3_N | Output | T21 |
| J3_8 | XCVR_0_RX3_N | Input | R19 |

| PIN # | Pin name | Description | Ball |
|--------------|------------------|--------------------|-------------|
| J3_9 | XCVR_0_TX3_P | Output | T22 |
| J3_10 | XCVR_0_RX3_P | Input | R20 |
| J3_11 | GND | Ground | |
| J3_12 | GND | Ground | |
| J3_13 | XCVR_0_TX2_N | Output | P21 |
| J3_14 | XCVR_0_RX2_N | Input | M21 |
| J3_15 | XCVR_0_TX2_P | Output | P22 |
| J3_16 | XCVR_0_RX2_P | Input | M22 |
| J3_17 | GND | Ground | |
| J3_18 | GND | Ground | |
| J3_19 | XCVR_0A_REFCLK_N | Input | L20 |
| J3_20 | XCVR_0B_REFCLK_N | Input | N20 |
| J3_21 | XCVR_0A_REFCLK_P | Input | L19 |
| J3_22 | XCVR_0B_REFCLK_P | Input | N19 |
| J3_23 | GND | Ground | |
| J3_24 | GND | Ground | |
| J3_25 | XCVR_0C_REFCLK_N | Input | J20 |
| J3_26 | GND | Ground | |
| J3_27 | XCVR_0C_REFCLK_P | Input | J19 |
| J3_28 | GND | Ground | |
| J3_29 | GND | Ground | |
| J3_30 | GND | Ground | |
| J3_31 | XCVR_0_TX1_N | Output | H21 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J3_32 | XCVR_0_RX1_N | Input | K21 |
| J3_33 | XCVR_0_TX1_P | Output | H22 |
| J3_34 | XCVR_0_RX1_P | Input | K22 |
| J3_35 | GND | Ground | |
| J3_36 | GND | Ground | |
| J3_37 | XCVR_0_TX0_N | Output | F21 |
| J3_38 | XCVR_0_RX0_N | Input | G19 |
| J3_39 | XCVR_0_TX0_P | Output | F22 |
| J3_40 | XCVR_0_RX0_P | Input | G20 |
| J3_41 | GND | Ground | |
| J3_42 | GND | Ground | |
| J3_43 | GPIO16_N | I/O | E18 |
| J3_44 | GPIO21_N | I/O | D20 |
| J3_45 | GPIO16_P | I/O | D18 |
| J3_46 | GPIO21_P | I/O | D21 |
| J3_47 | GPIO15_N | I/O | C17 |
| J3_48 | GPIO23_N | I/O | D22 |
| J3_49 | GPIO15_P | I/O | B17 |
| J3_50 | GPIO23_P | I/O | C22 |
| J3_51 | GPIO8_N | I/O | H17 |
| J3_52 | GPIO22_N | I/O | B22 |
| J3_53 | GPIO8_P | I/O | G17 |
| J3_54 | GPIO22_P | I/O | B21 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J3_55 | GPIO11_N | I/O | F16 |
| J3_56 | GPIO18_N | I/O | C20 |
| J3_57 | GPIO11_P | I/O | F17 |
| J3_58 | GPIO18_P | I/O | C19 |
| J3_59 | GPIO14_N | I/O | D19 |
| J3_60 | GPIO4_N | I/O | C15 |
| J3_61 | GPIO14_P | I/O | E19 |
| J3_62 | GPIO4_P | I/O | C14 |
| J3_63 | GPIO185_N | I/O | H13 |
| J3_64 | GPIO12_N | I/O | D17 |
| J3_65 | GPIO185_P | I/O | G13 |
| J3_66 | GPIO12_P | I/O | C16 |
| J3_67 | GPIO7_N | I/O | H15 |
| J3_68 | GPIO9_N | I/O | E14 |
| J3_69 | GPIO7_P | I/O | G15 |
| J3_70 | GPIO9_P | I/O | E15 |
| J3_71 | GPIO6_N | I/O | G14 |
| J3_72 | GPIO20_N | I/O | A21 |
| J3_73 | GPIO6_P | I/O | F15 |
| J3_74 | GPIO20_P | I/O | A20 |
| J3_75 | GPIO10_N | I/O | D16 |
| J3_76 | GPIO19_N | I/O | B19 |
| J3_77 | GPIO10_P | I/O | E16 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J3_78 | GPIO19_P | I/O | B20 |
| J3_79 | GPIO3_N | I/O | B14 |
| J3_80 | GPIO17_N | I/O | B18 |
| J3_81 | GPIO3_P | I/O | B13 |
| J3_82 | GPIO17_P | I/O | A18 |
| J3_83 | GPIO1_N | I/O | A12 |
| J3_84 | GPIO5_N | I/O | B15 |
| J3_85 | GPIO1_P | I/O | A13 |
| J3_86 | GPIO5_P | I/O | A15 |
| J3_87 | GPIO2_N | I/O | D14 |
| J3_88 | GPIO13_N | I/O | A17 |
| J3_89 | GPIO2_P | I/O | D13 |
| J3_90 | GPIO13_P | I/O | A16 |

7.2.5. Connector J4 overview and pinouts

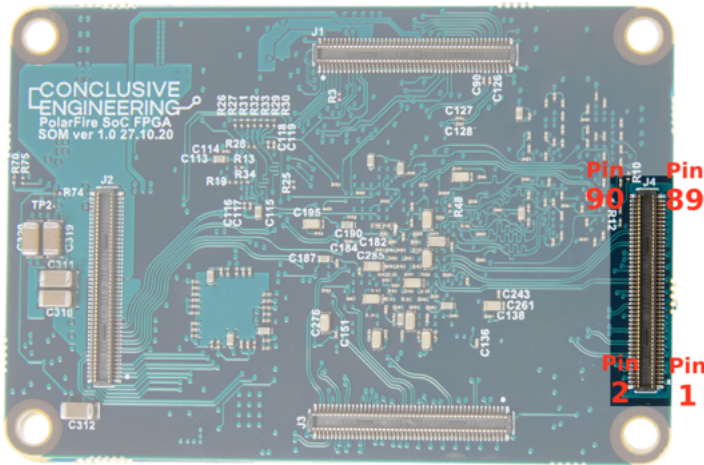


Fig. 7.6 Connector J4 on RCHD-PF (bottom view).

Connector J4 exposes the following connectivity of the RCHD-PF:

- High Speed Input Output (HSIO)

Table 74 SoM Board-to-Board Connector J4

| PIN # | Pin name | Description | Ball |
|-------|----------|-------------|------|
| J4_1 | HSIO68_P | I/O | W21 |
| J4_2 | HSIO74_P | I/O | U19 |
| J4_3 | HSIO68_N | I/O | V21 |
| J4_4 | HSIO74_N | I/O | U18 |
| J4_5 | GND | Ground | |
| J4_6 | GND | Ground | |
| J4_7 | HSIO72_P | I/O | V20 |
| J4_8 | HSIO66_P | I/O | W22 |
| J4_9 | HSIO72_N | I/O | V19 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J4_10 | HSIO66_N | I/O | V22 |
| J4_11 | GND | Ground | |
| J4_12 | GND | Ground | |
| J4_13 | HSIO79_P | I/O | W19 |
| J4_14 | HSIO69_P | I/O | AA21 |
| J4_15 | HSIO79_N | I/O | W18 |
| J4_16 | HSIO69_N | I/O | AA22 |
| J4_17 | GND | Ground | |
| J4_18 | GND | Ground | |
| J4_19 | HSIO67_P | I/O | Y20 |
| J4_20 | HSIO80_P | I/O | Y19 |
| J4_21 | HSIO67_N | I/O | Y21 |
| J4_22 | HSIO80_N | I/O | Y18 |
| J4_23 | GND | Ground | |
| J4_24 | GND | Ground | |
| J4_25 | HSIO76_P | I/O | V17 |
| J4_26 | HSIO71_P | I/O | AB21 |
| J4_27 | HSIO76_N | I/O | V16 |
| J4_28 | HSIO71_N | I/O | AA20 |
| J4_29 | GND | Ground | |
| J4_30 | GND | Ground | |
| J4_31 | HSIO85_P | I/O | Y15 |
| J4_32 | HSIO83_P | I/O | W16 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J4_33 | HSIO85_N | I/O | AA15 |
| J4_34 | HSIO83_N | I/O | W17 |
| J4_35 | GND | Ground | |
| J4_36 | GND | Ground | |
| J4_37 | HSIO75_P | I/O | T16 |
| J4_38 | HSIO73_P | I/O | T17 |
| J4_39 | HSIO75_N | I/O | R16 |
| J4_40 | HSIO73_N | I/O | U17 |
| J4_41 | GND | Ground | |
| J4_42 | GND | Ground | |
| J4_43 | HSIO70_P | I/O | AB19 |
| J4_44 | HSIO91_P | I/O | U15 |
| J4_45 | HSIO70_N | I/O | AB20 |
| J4_46 | HSIO91_N | I/O | T15 |
| J4_47 | GND | Ground | |
| J4_48 | GND | Ground | |
| J4_49 | HSIO78_P | I/O | AB18 |
| J4_50 | HSIO77_P | I/O | R15 |
| J4_51 | HSIO78_N | I/O | AA18 |
| J4_52 | HSIO77_N | I/O | R14 |
| J4_53 | GND | Ground | |
| J4_54 | GND | Ground | |
| J4_55 | HSIO81_P | I/O | AB17 |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J4_56 | HSIO90_P | I/O | V14 |
| J4_57 | HSIO81_N | I/O | AA17 |
| J4_58 | HSIO90_N | I/O | V15 |
| J4_59 | GND | Ground | |
| J4_60 | GND | Ground | |
| J4_61 | HSIO82_P | I/O | AA16 |
| J4_62 | HSIO93_P | I/O | U14 |
| J4_63 | HSIO82_N | I/O | Y16 |
| J4_64 | HSIO93_N | I/O | U13 |
| J4_65 | GND | Ground | |
| J4_66 | GND | Ground | |
| J4_67 | HSIO87_P | I/O | Y14 |
| J4_68 | HSIO95_P | I/O | R12 |
| J4_69 | HSIO87_N | I/O | W14 |
| J4_70 | HSIO95_N | I/O | T13 |
| J4_71 | GND | Ground | |
| J4_72 | GND | Ground | |
| J4_73 | HSIO84_P | I/O | AB14 |
| J4_74 | HSIO94_P | I/O | U12 |
| J4_75 | HSIO84_N | I/O | AB15 |
| J4_76 | HSIO94_N | I/O | T12 |
| J4_77 | GND | Ground | |
| J4_78 | GND | Ground | |

| PIN # | Pin name | Description | Ball |
|--------------|-----------------|--------------------|-------------|
| J4_79 | HSIO89_P | I/O | W13 |
| J4_80 | HSIO92_P | I/O | W12 |
| J4_81 | HSIO89_N | I/O | Y13 |
| J4_82 | HSIO92_N | I/O | V12 |
| J4_83 | GND | Ground | |
| J4_84 | GND | Ground | |
| J4_85 | HSIO86_P | I/O | AA13 |
| J4_86 | HSIO88_P | I/O | AA12 |
| J4_87 | HSIO86_N | I/O | AB13 |
| J4_88 | HSIO88_N | I/O | AB12 |
| J4_89 | GND | Ground | |
| J4_90 | GND | Ground | |

8. Electrical Specifications

8.1. Absolute Maximum Ratings

Table 8.1 Absolute maximum ratings

| Pin | Min | Max | Units | Comments |
|----------|------|------|-------|--|
| 3V3 | -0.5 | 3.6 | V | Main power supply pins |
| VBUS | -0.3 | 5.5 | V | |
| USB pins | -0.5 | 6 | V | |
| MDI | -0.3 | 6.5 | V | |
| GPIO | -0.5 | 3.8 | V | Maximum DC input VIN voltage on GPIO |
| HSIO | -0.5 | 2.2 | V | Maximum DC input VIN voltage on HSIO |
| XCVR | -0.5 | 1.26 | V | Transceiver receiver absolute input voltage |
| XCVR CLK | -0.5 | 3.6 | V | Transceiver reference clock absolute input voltage |
| XCVR CLK | -0.5 | 3.6 | V | Transceiver reference clock absolute input voltage |

Maximum power consumption of the RCHD-PF is 30W, without additional loads on the outgoing power supply pins.

8.2. Recommended Operating Conditions

Table 8.2 Recommended operating conditions

| Pin | Min | Typ | Max | Units | Comments |
|------|-------|-----|-------|-------|------------------------|
| 3V3 | 3.135 | 3.3 | 3.465 | V | Main power supply pins |
| VBUS | 0 | 5.0 | 5.5 | V | |

| Pin | Min | Typ | Max | Units | Comments |
|----------|-----|-----|-----|-------|----------|
| USB pins | 0 | | 3.6 | V | |

8.3. Output Power Supplies

RCHD-PF exposes five general purpose switching power supplies. Table below shows max current from each power rail.

Table 8.3 Output power supplies

| Voltage (V) | Max available current (mA) | Pins |
|-------------|----------------------------|-----------------------------------|
| 1.05 | 500 | J1_28, J1_30, J1_32, J1_34, J1_36 |
| 1.1 | 100 | J1_58, J1_60, J1_62, J1_64, J1_66 |
| 1.8 | 100 | J1_38, J1_40, J1_42, J1_44, J1_46 |
| 2.5 | 100 | J1_48, J1_50, J1_52, J1_54, J1_56 |
| 5 | 1500 | J1_18, J1_20, J1_22, J1_24, J1_26 |

9. Environmental Specifications

Table 9.1 Environmental Specifications

| Parameter | Min | Max |
|--|--------|---------|
| Operating temperature range | -40° C | +85° C |
| Storage Temperature (eMMC flash memory is the limiting device) | -40° C | +85° C |
| Junction temperature SoC | -55° C | +135° C |

10. SOM Dimensions

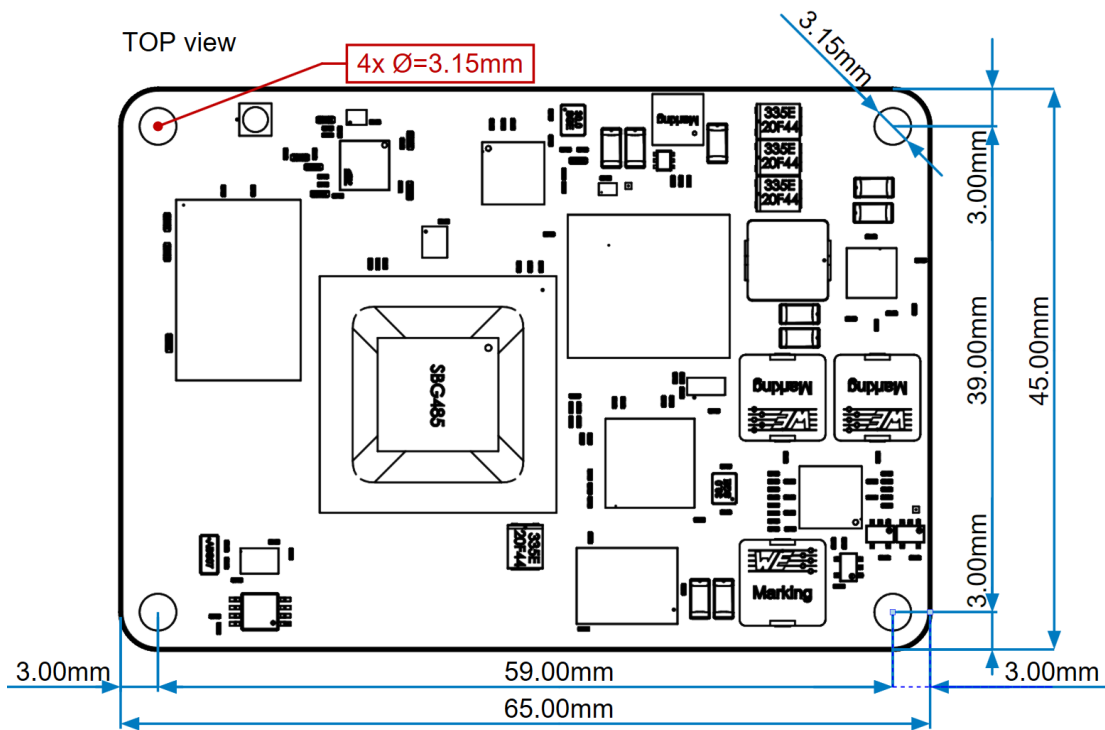


Fig. 10.1 RCHD-PF Top View Mechanics in millimeters

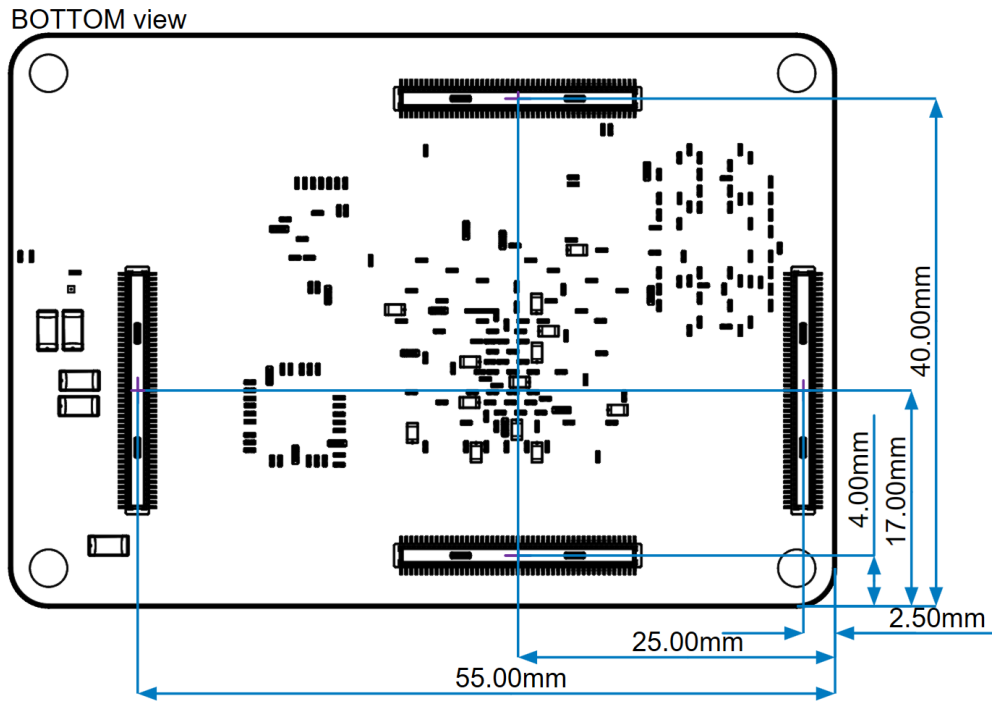


Fig. 10.2 RCHD-PF Bottom View Mechanics in millimeters

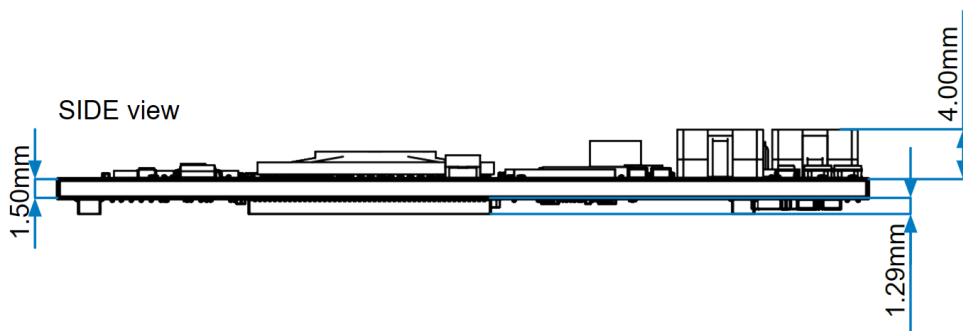
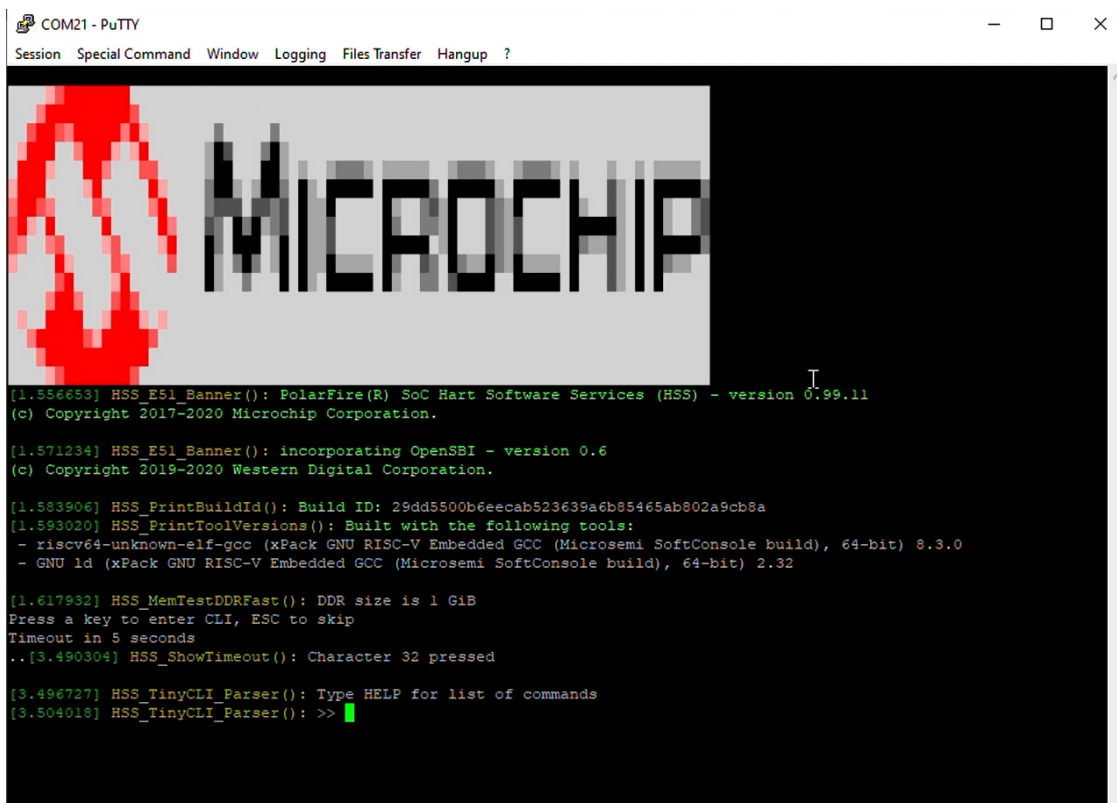


Fig. 10.3 RCHD-PF Side View Mechanics in millimeters

11. Boot process

11.1. Intro

RCHD-PF comes with a pre-installed HSS (Haart Software Services) on boot flash. The built-in MMC memory contains a pre-programmed Linux environment.



```
COM21 - PuTTY
Session Special Command Window Logging Files Transfer Hangup ?

[1.556653] HSS_E51_Banner(): PolarFire(R) SoC Haart Software Services (HSS) - version 0.99.11
(c) Copyright 2017-2020 Microchip Corporation.

[1.571234] HSS_E51_Banner(): incorporating OpenSBI - version 0.6
(c) Copyright 2019-2020 Western Digital Corporation.

[1.583906] HSS_PrintBuildId(): Build ID: 29dd5500b6eecab523639a6b85465ab802a9cb8a
[1.593020] HSS_PrintToolVersions(): Built with the following tools:
- riscv64-unknown-elf-gcc (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit) 8.3.0
- GNU ld (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit) 2.32

[1.617932] HSS_MemTestDDRFast(): DDR size is 1 GiB
Press a key to enter CLI, ESC to skip
Timeout in 5 seconds
..[3.490304] HSS_ShowTimeout(): Character 32 pressed

[3.496727] HSS_TinyCLI_Parser(): Type HELP for list of commands
[3.504018] HSS_TinyCLI_Parser(): >> █
```

Fig. 11.1 Haart Software Services

11.1.1. Boot Prerequisites

- RCHD-PF with RCHD-PF-EVAL.
- HSS service on eNVM
- USB cable

11.1.2. Boot Instructions

1. Open a terminal on HSS Com Port, turn on the board and enter to HSS CLI by pressing any key during a 5 second timeout.
2. Run USB mass storage: USBDMSC



```

[1.556640] HSS_E51_Banner(): PolarFire(R) SoC Hart Software Services (HSS) - version 0.99
.11
(c) Copyright 2017-2020 Microchip Corporation.

[1.571220] HSS_E51_Banner(): incorporating OpenSBI - version 0.6
(c) Copyright 2019-2020 Western Digital Corporation.

[1.593892] HSS_PrintBuildId(): Build ID: daad750586bb19ba9f594dbafbc3a07784b68a0c
[1.593007] HSS_PrintToolVersions(): Built with the following tools:
- riscv64-unknown-elf-gcc.exe (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit) 8.3.0
- GNU ld (xPack GNU RISC-V Embedded GCC (Microsemi SoftConsole build), 64-bit) 2.32

[1.618266] HSS_MemTestDDRFast(): DDR size is 1 GiB
Press a key to enter CLI, ESC to skip
Timeout in 5 seconds
...[4.211468] HSS_ShowTimeout(): Character 32 pressed

[4.217891] HSS_TinyCLI_Parser(): Type HELP for list of commands
[4.225183] HSS_TinyCLI_Parser(): >> USBDMSC
Waiting for USB Host to connect... (CTRL-C to quit)
USB Host connected. Waiting for disconnect... (CTRL-C to quit)
0 bytes written, 4165120 bytes read

```

Fig. 11.2 USB host connection

For a new eMMC proceed with the following configuration steps. If eMMC is already configured, please skip to point 6.

1. Delete and format all partitions.
2. Create two partitions:
 - 10MB partition for BIOS BOOT (GUID: 21686148-6449-6E6F-744E-656564454649)
 - Allocate the remaining space as a Microsoft basic data (GUID: EBD0A0A2-B9E5-4433-87C0-68B6B72699C7)
3. Write a file with BIOS boot payload to first partition (for example using the 'dd' commandline program). In Conclusive repositories, the file is named payload.bin
4. On the second partition please write two files from the Conclusive RCHD-PF repositories: fitimage.fit and uEnv.txt
5. Exit HSS and boot linux.

12. Ordering information

RCHD-PF can be ordered directly from our website, at <https://store.conclusive.pl>

RCHD-PF comes in different configurations. The variable elements include the LPDDR4, eMMC, SoC version, WiFi option and VCC core voltage. Available configurations are presented in the following graph:

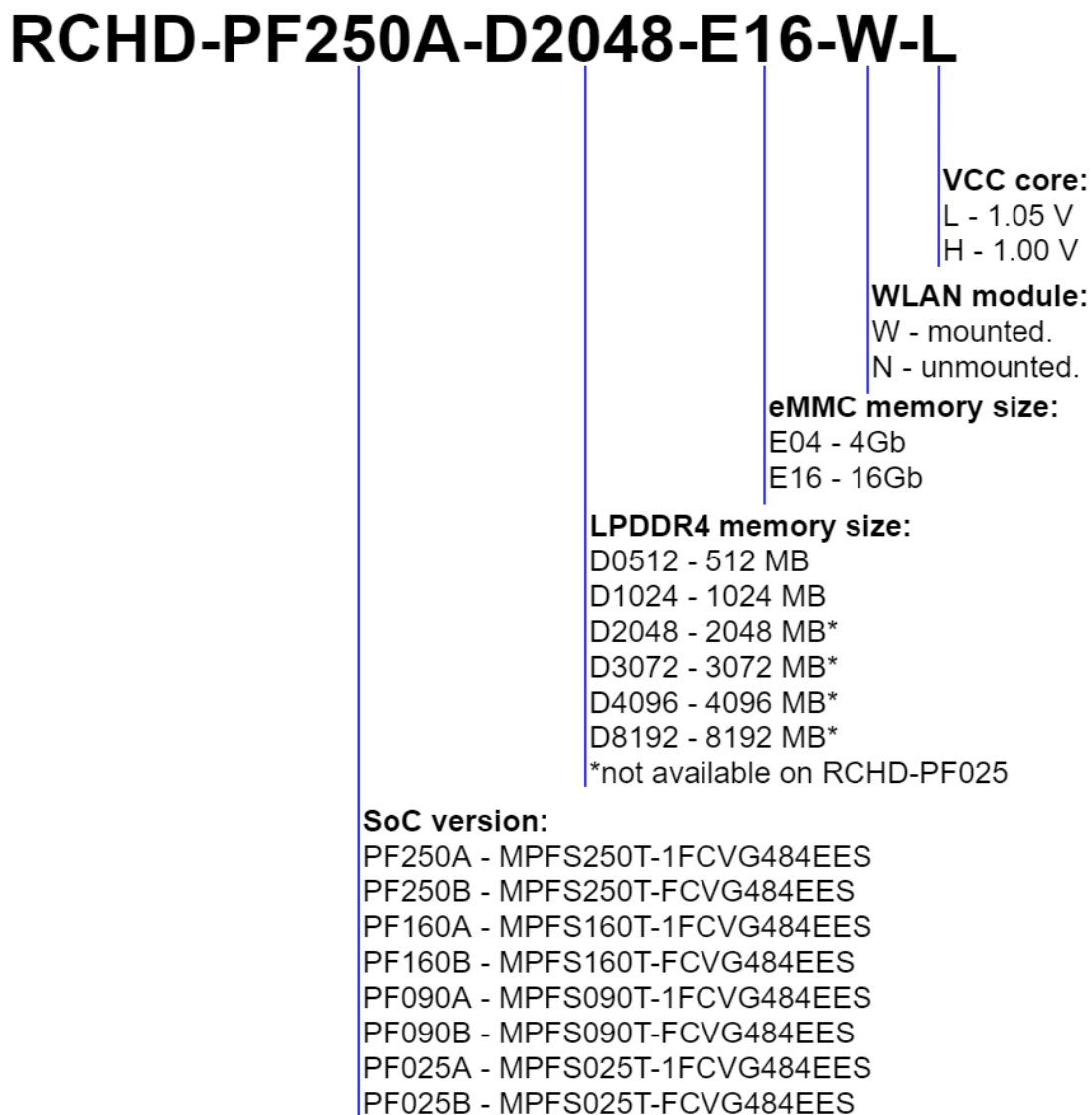


Fig. 12.1 Ordering information.

