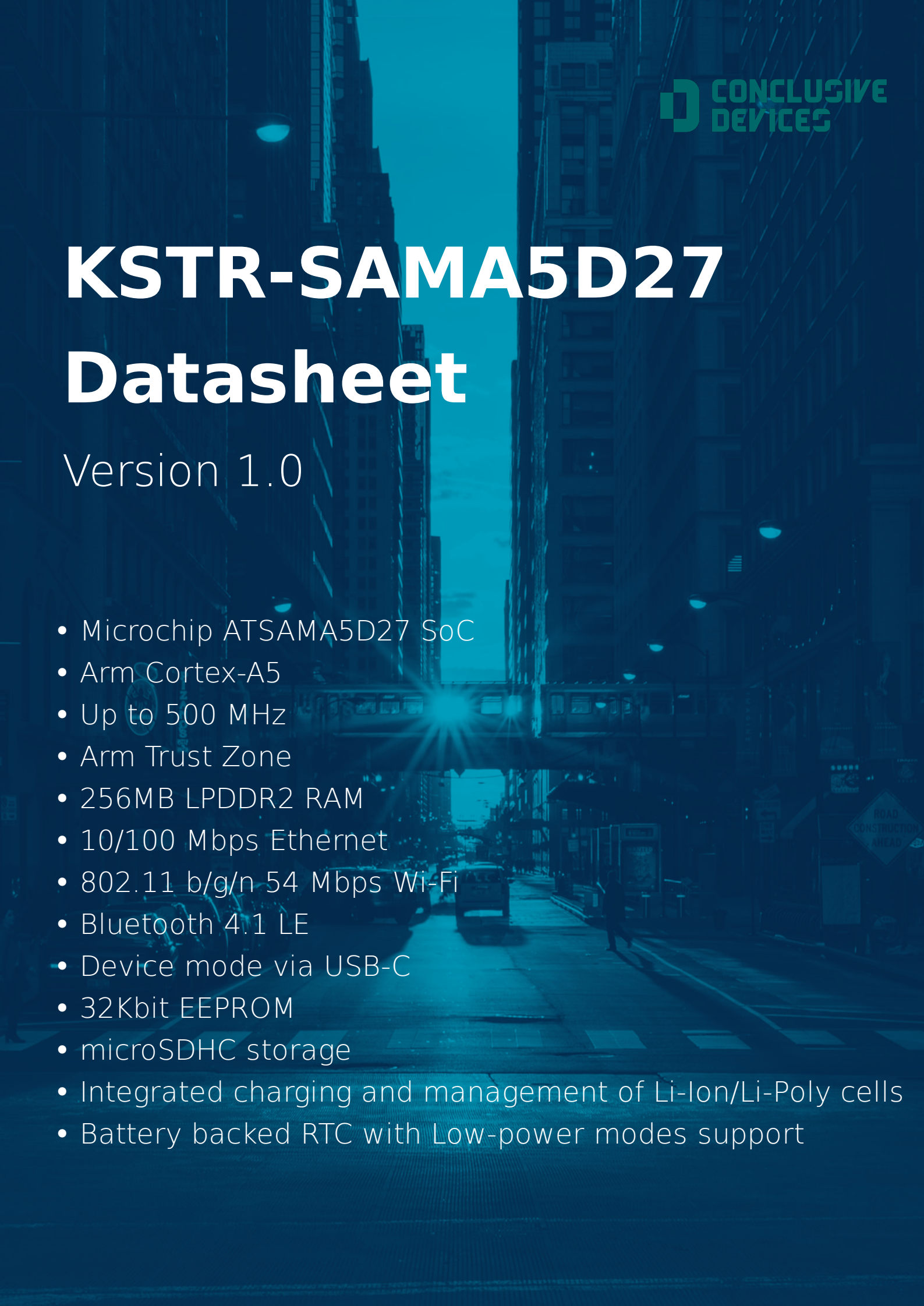


KSTR-SAMA5D27 Datasheet

Version 1.0

- Microchip ATSAMA5D27 SoC
- Arm Cortex-A5
- Up to 500 MHz
- Arm Trust Zone
- 256MB LPDDR2 RAM
- 10/100 Mbps Ethernet
- 802.11 b/g/n 54 Mbps Wi-Fi
- Bluetooth 4.1 LE
- Device mode via USB-C
- 32Kbit EEPROM
- microSDHC storage
- Integrated charging and management of Li-Ion/Li-Poly cells
- Battery backed RTC with Low-power modes support

Table of Contents:

1. List of tables

2. Revision history

Table 2.1 Revision History

Revision	Date	Notes
1	Feb 26, 2021	Initial - Preliminary
1.1	Mar 16, 2021	Add summary of boot process
1.2	Apr 1, 2022	Review and detailed update of all sections

3. Overview

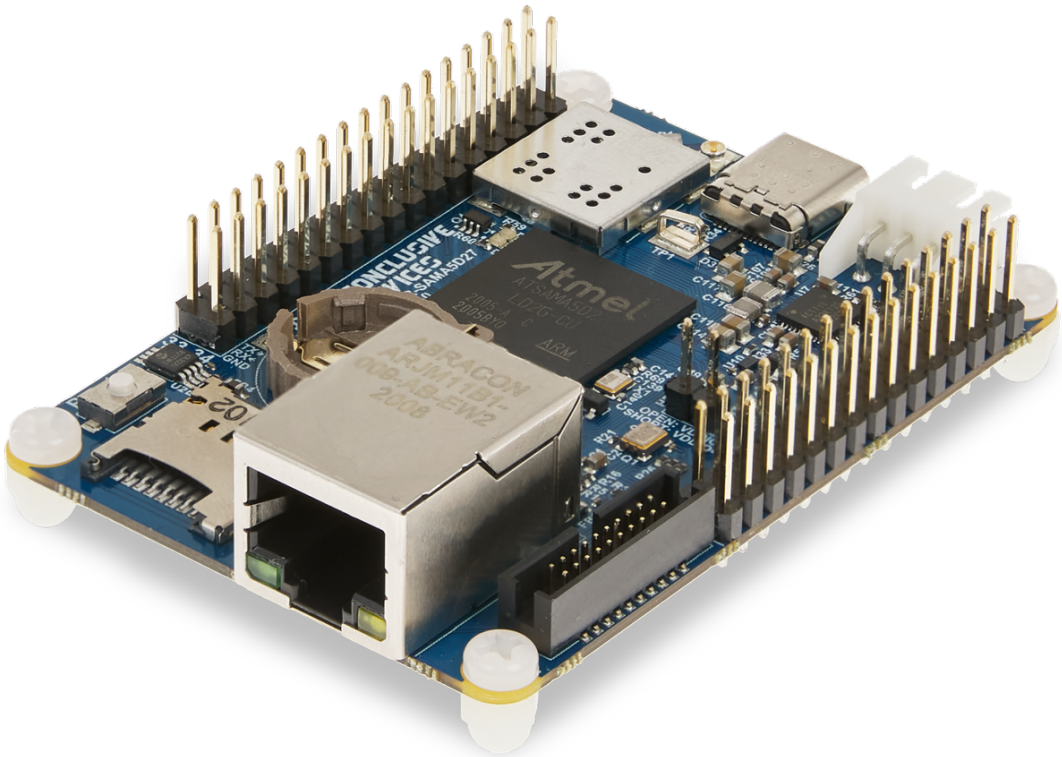


Fig. 3.1 KSTR-SAMA5D27 module.

The Conclusive Engineering Kestrel KSTR-SAMA5D27 is a Single Board Computer featuring a ATSAMA5D27, ARM® Cortex®-A5 based System on Chip from Microchip. Delivering around 785 DMIPS at 500MHz, this is one of the leanest SoCs capable of running a full Linux or FreeBSD operating system.

Kestrel is designed for long battery operation and energy efficiency. It can be powered directly by a Li-Ion or Li-Poly battery thanks to an integrated battery management system. It's capable of several deep sleep states, and has a real time clock powered by a separate on-board battery, that can be used to manage the board's power cycles and wake/sleep timers.

Kestrel is capable of running realtime workloads, and offers great connectivity options for external devices with a total of over 60 IO lanes and Fast Ethernet with a dedicated controller. All this on a PCB that's smaller than a credit card.

It also delivers advanced security (Arm TrustZone® , tamper detection, secure data storage, secure boot) and high-performance crypto accelerators (AES, SHA and TRNG).

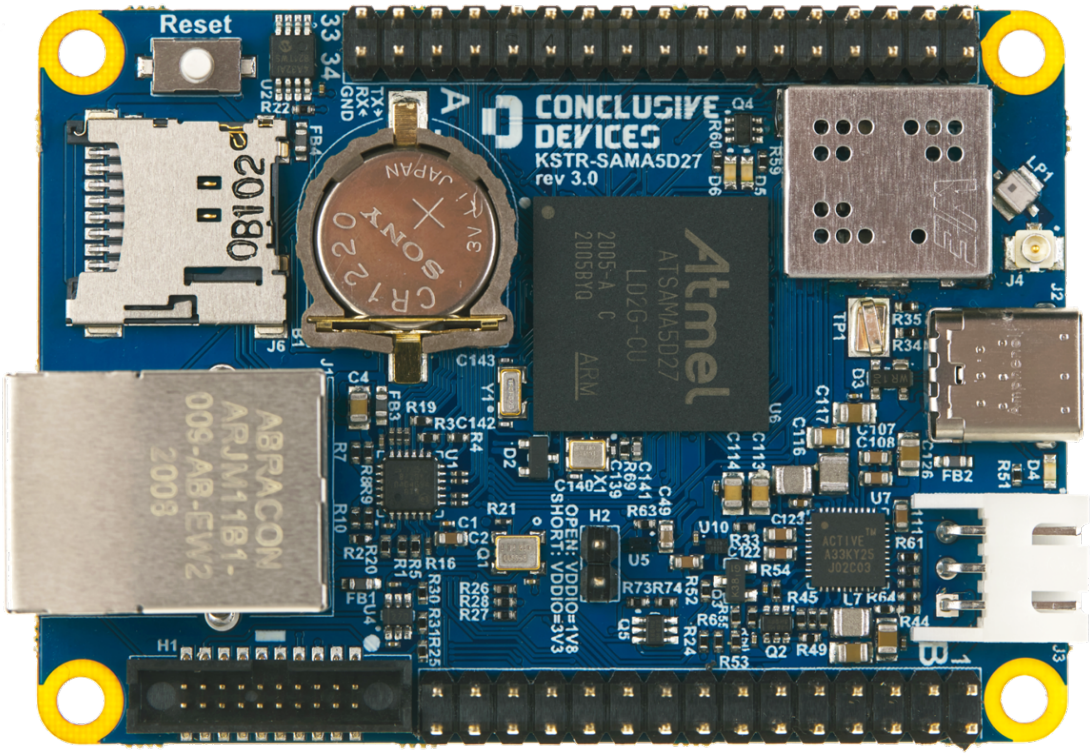


Fig. 3.2 KSTR-SAMA5D27 board TOP view.

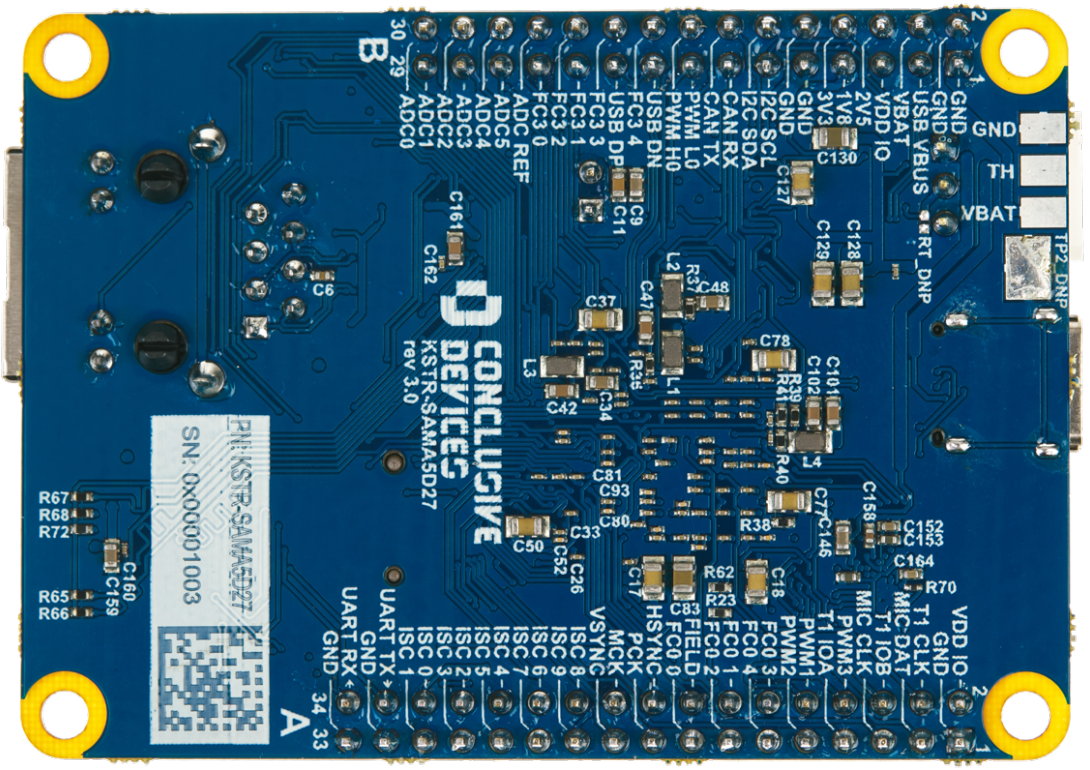


Fig. 3.3 KSTR-SAMA5D27 board BOTTOM view.

4. Features of KSTR-SAMA5D27

Microchip ATSAMA5D27 microprocessor features:

- 32-bit ARMv7 Cortex-A5 500MHz core processor
- Most extensive variant with 361 ball BGA socket
- **Memory Architecture:**
    - Memory Management Unit
    - 256MB LPDDR2 SDRAM - up to 2Gbit
    - L1 Cache Memory (Instructions) - 32KB
    - L1 Cache Memory (Data) - 32KB
    - L2 Cache Memory - 128KB
    - Scrambled Internal SRAM - 128KB
    - Internal ROM - 160KB
- **Ultra-Low Power Consumption:**
    - Low power consumption architecture for extended battery life
    - <200µA retention mode with fast wake-up
    - 5uA in backup mode
- **State-of-the-Art Security:**
    - ARM TrustZone
    - Secure Boot
    - Execution of encrypted code with an “on-the-fly” encryption-decryption process
    - Integrity Check Monitor of the memory content
    - Hardware encryption engine
    - Tamper pins and secure key storage
- NEON™ Media Processing Engine
- ETM/ETB 8KB
- Embedded Real-Time Clock
- Battery-backed Low-Power 5KB SRAM
- Wide -40 °C to 105 °C Temperature Range

KSTR-SAMA5D27 features:

- **Wireless connectivity:**
    - 802.11 b/g/n MAC WiFi
    - Bluetooth 4.1 LE
    - u.fl antenna connector
- **Wired connectivity:**
    - USB 2.0 High-Speed Device mode (USB Type-C connector)

- 10/100 Mbit Ethernet (RJ-45 connector)

· **Storage:**
- Micro-SD card slot - SD 3.0 SDSC, SDHC, SDXC up to UHS-I SDR104
- 8KB EEPROM

· **Battery support:**
- Single cell Li-Ion/Li-Poly battery connector
- Li-Ion/Li-Poly charging capability with thermal control
- Undervoltage/Overvoltage protection
- Automatic main power switching and failover between USB-C and battery

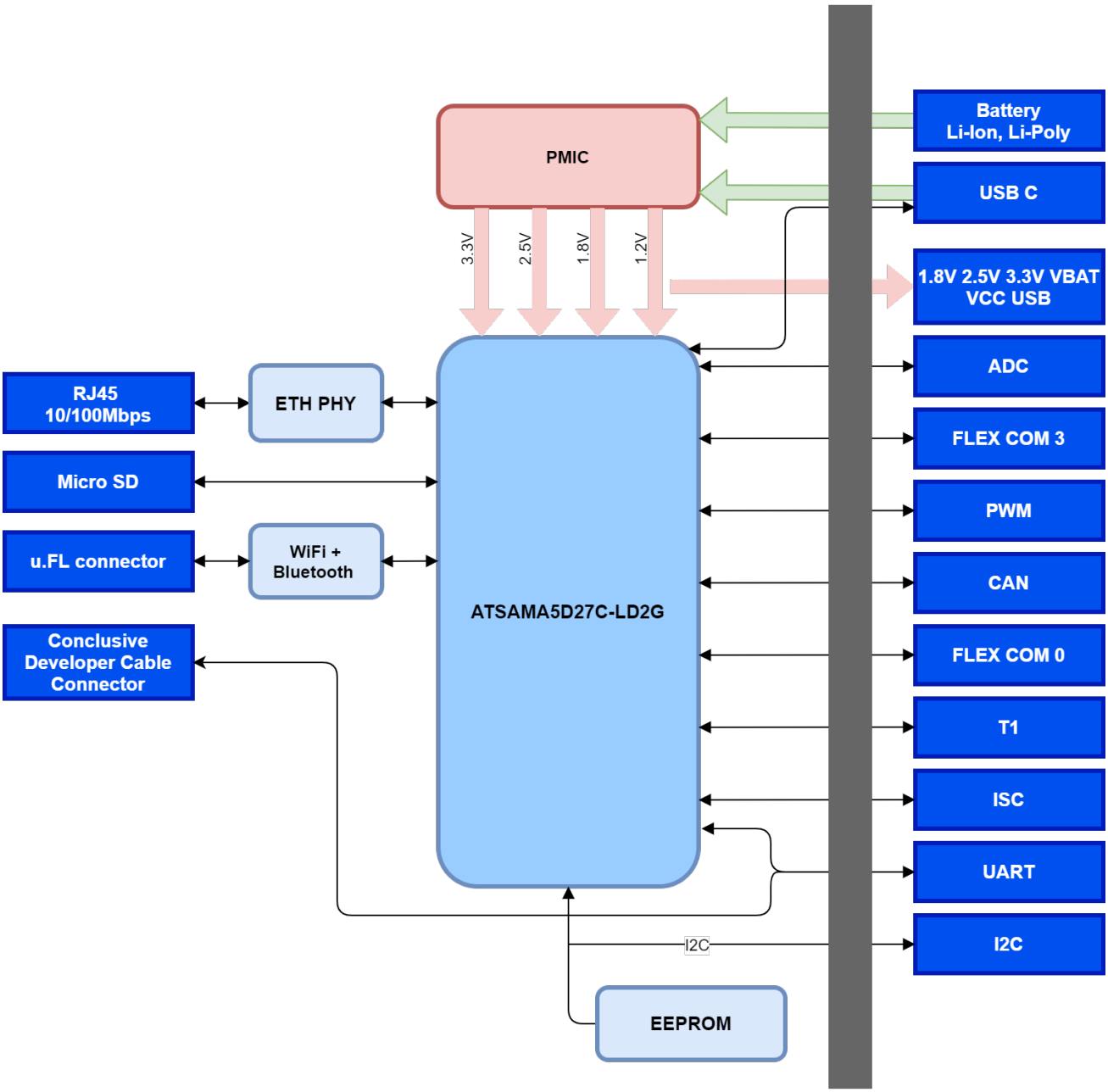
· CR1220 battery holder providing RTC/Low-Power SRAM backup power

· Dual I/O voltage support (1.8V/3.3V selectable)

· **Two I/O headers (2x17 + 2x15) featuring:**
- 6x ADC channels
- 2x FLEXCOM (UART, SPI, TWI)
- 4x PWM Single Ended
- 1x PWM Differential
- 1x CAN
- 1x I2C
- 1x Debug UART
- 1x Image Sensor Controller (ISC)
- 1x Timer/Counter
- 1x USB High-Speed host
- 1x PDMIC audio input
- 1x 3.3V power output
- 1x 2.5V power output
- 1x 1.8V power output
- 1x Direct Li-Ion/Li-Poly battery power output
- 1x 5V USB VBUS power output
- 1x IO voltage power output

· **Conclusive Developer Connector providing access to:**
- JTAG port
- Debug UART
- System I2C bus

5. Block diagram



6. Main hardware components

This section summarizes the main hardware building blocks of the KSTR-SAMA5D27.

6.1. ATSAMA5D27 SoC

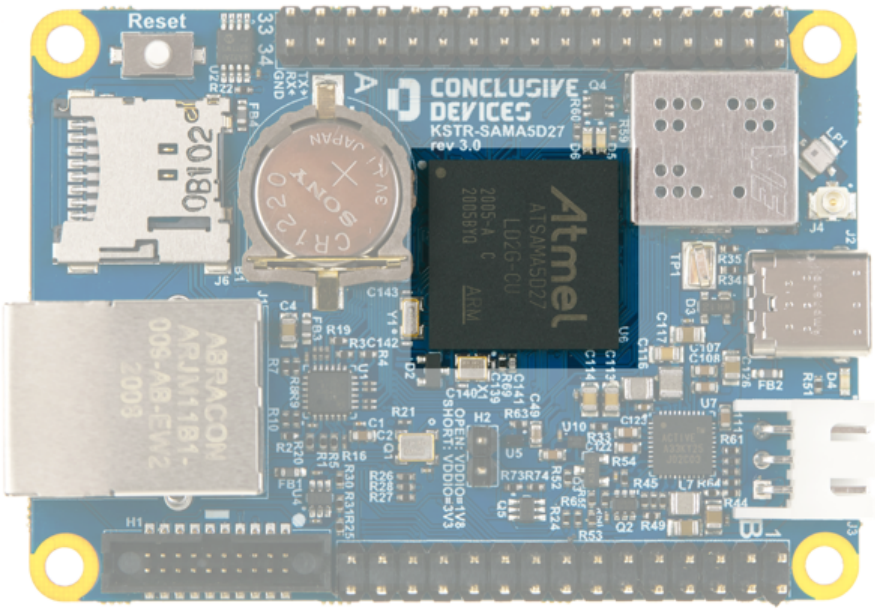


Fig. 6.1 ATSAMA5D27 SoC location

The ATSAMA5D27 is a System-on-Chip (SoC) that is composed of:

- an Arm® Cortex®-A5 processor-based ATSAMA5D27 MPU
- 256MB LPDDR2 SDRAM memory, 2Gbit

Integrating the MPU with SDRAM memory allows for reduced overall PCB complexity, better EMI, ESD and signal integrity characteristics.

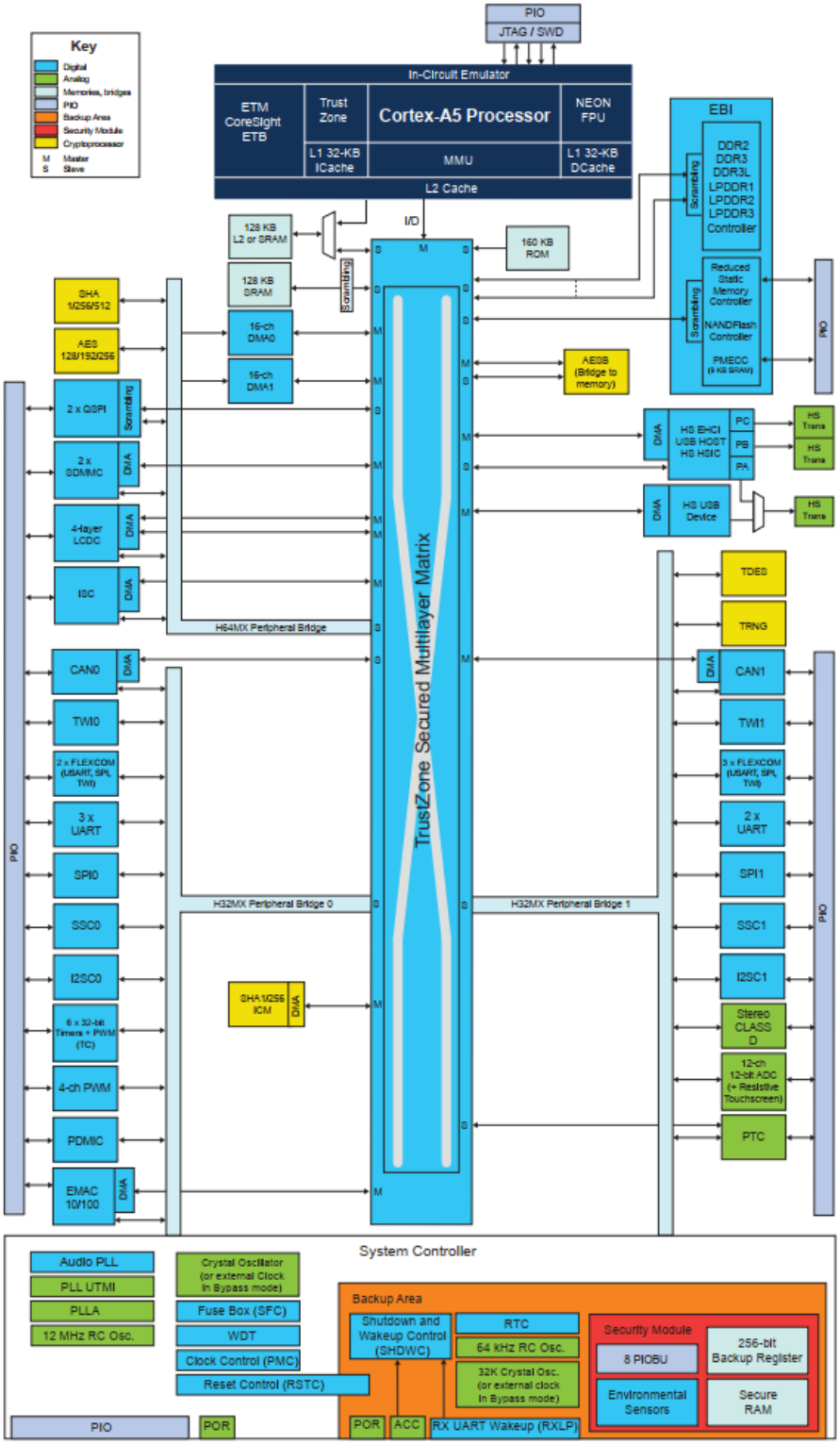


Fig. 6.2 ATSAMA5D27 series block diagram.

6.2. ACT8945A ActivePMU PMIC

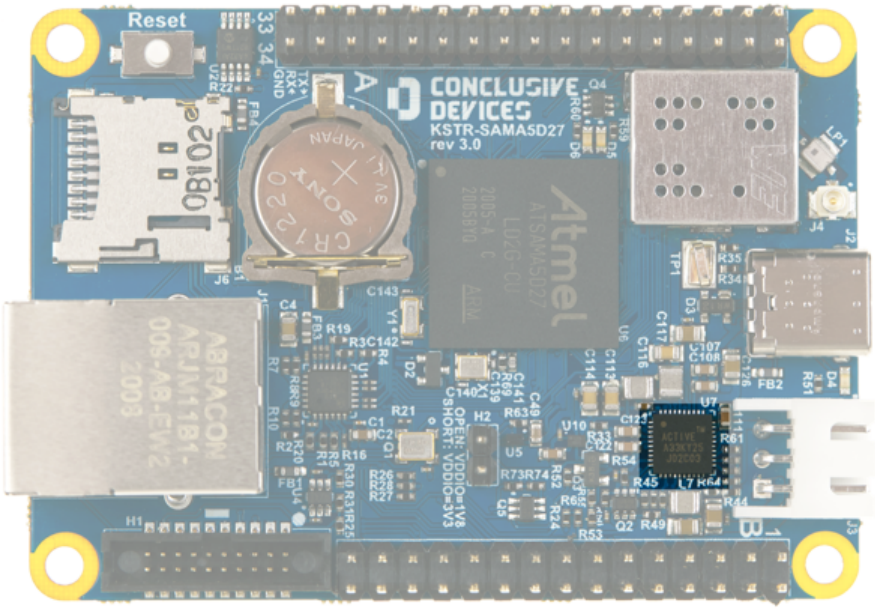


Fig. 6.3 ACT8945A PMIC location

KSTR-SAMA5D27 is powered using the ACT8945A PMIC - complete, cost effective, highly efficient ActivePMU power management solution. This device integrates the ActivePath complete battery charging and management system with seven output power supply channels.

ACT8945A provides fine control over the Li-Ion/Li-Poly charging process and state of the power outputs. It is available via the I2C interface connected directly to the system I2C bus of KSTR-SAMA5D27.

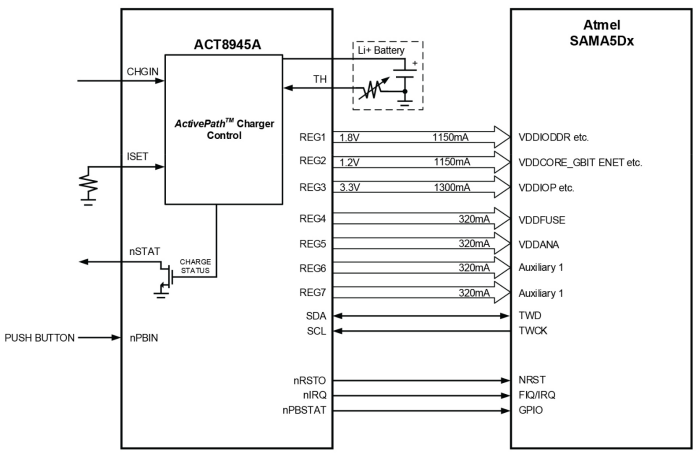


Fig. 6.4 ACT8945A PMIC block diagram and connectivity to ATSAMA5D27 SoC.

6.3. WiFi + Bluetooth

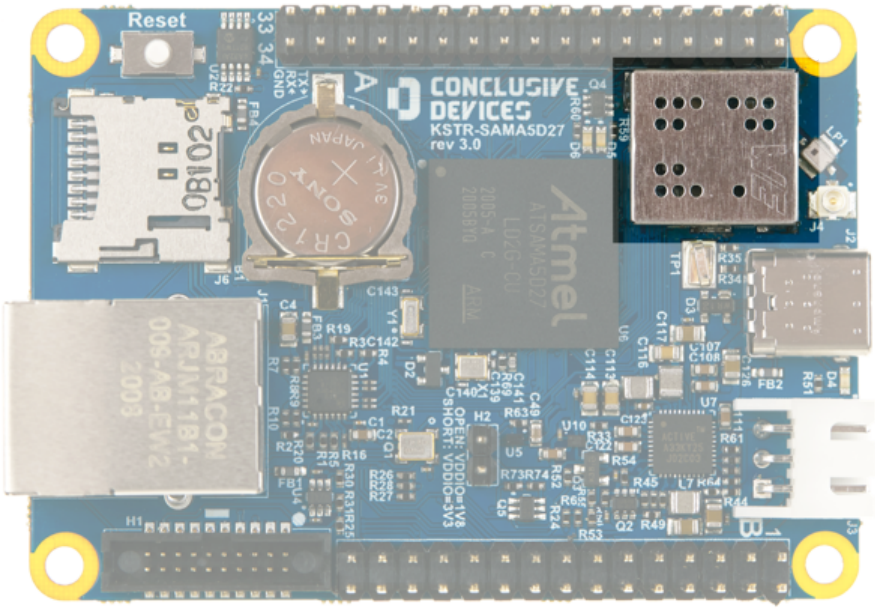


Fig. 6.5 Infineon CYW4343W location

The KSTR-SAMA5D27 contains a low power SDIO Wi-Fi + Bluetooth solution based on Infineon CYW4343W. It's connected to the ATSAMA5D2 SoC through SDMMC1 and FLEXCOM1 (UART) interfaces.

Key features:

- IEEE 802.11 b/g/n compliant
- Bluetooth Core Specification Version 4.1 compliant
- Bluetooth Class 1 or Class 2 transmitter
- TX power: up to +17.5 dBm (at pin)
- RX sensitivity: up to -88 dBm (at pin)
- Integrated support for antenna diversity
- Low power consumption
- Secure and signed software

6.4. Ethernet PHY

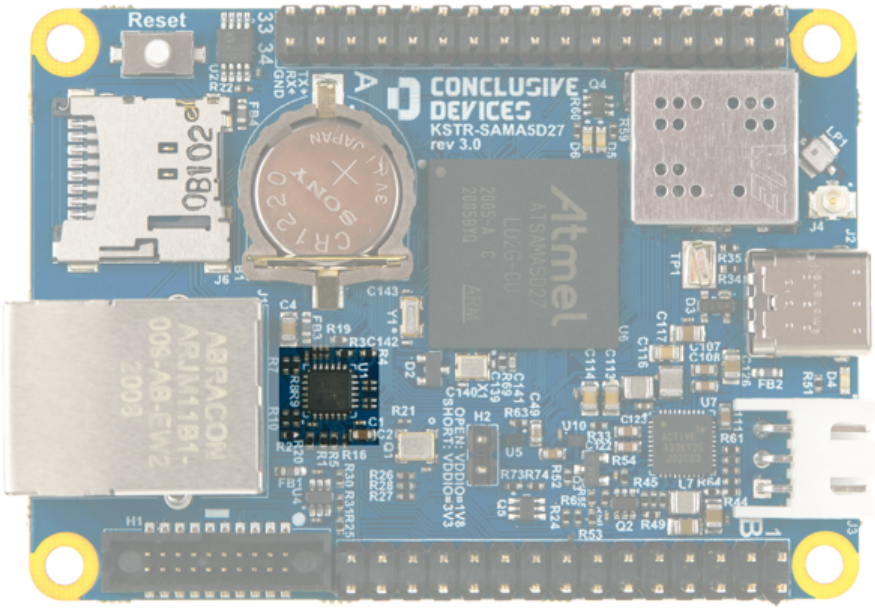


Fig. 6.6 ATSAMA5D27 SoC location

The KSTR-SAMA5D27 comes equipped with the LAN8720A from Microchip - low-power 10BASE-T/100BASE-TX physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards.

LAN8720A is configured to disable its internal 1.2V linear regulator. The necessary power is provided from the main PMIC instead. This enhances the low power capabilities of KSTR-SAMA5D27.

6.5. 24AA32A EEPROM

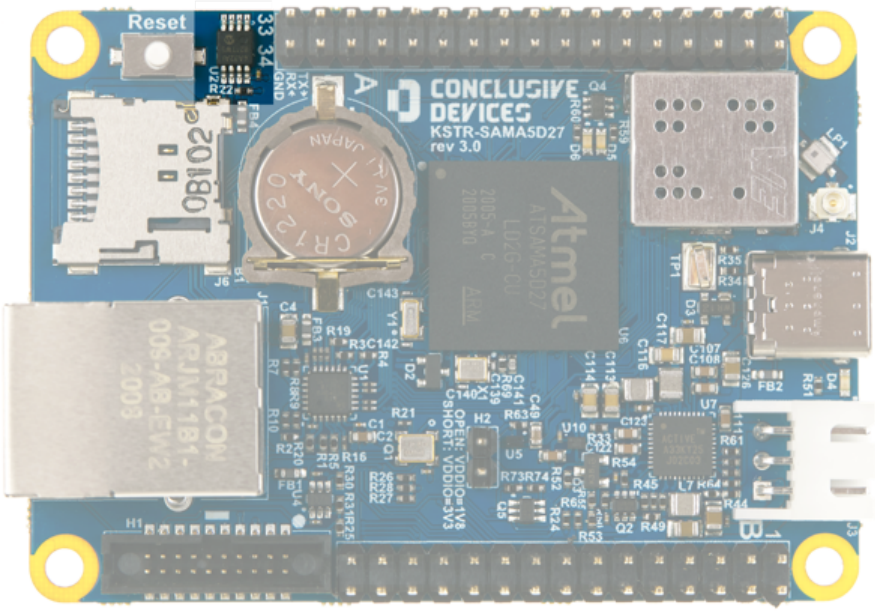


Fig. 6.7 24AA32A EEPROM location

The KSTR-SAMA5D27 has a built-in 32Kbit EEPROM 24AA32A chip, available via I2C. 400KHz frequency, 900ns latency. EEPROM holds unique board information, such as serial number or MAC address. The data is kept in a TLV format. To learn more, please visit our Wiki at:

https://wiki.conclusive.pl/bin/view/Main/Conclusive%20EEPROM%20format/

6.6. Reset Switch

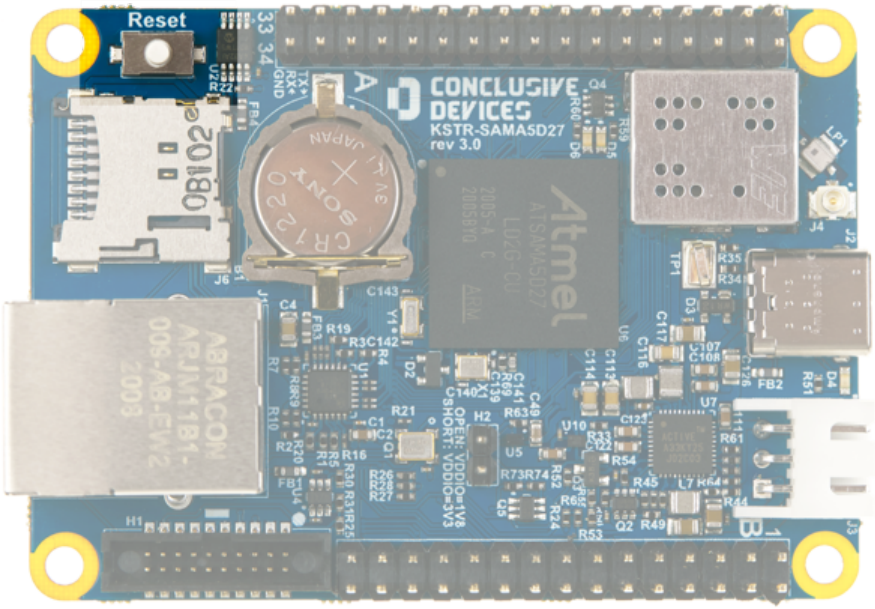


Fig. 6.8 Board reset switch location

A single reset switch. It's wired directly to the PMIC, pressing it causes a hard power cycle of the board. It causes the PMIC to cut power supply to the board components, performing a full power cycle of the board.

6.7. VDDIO Voltage Regulator Pins

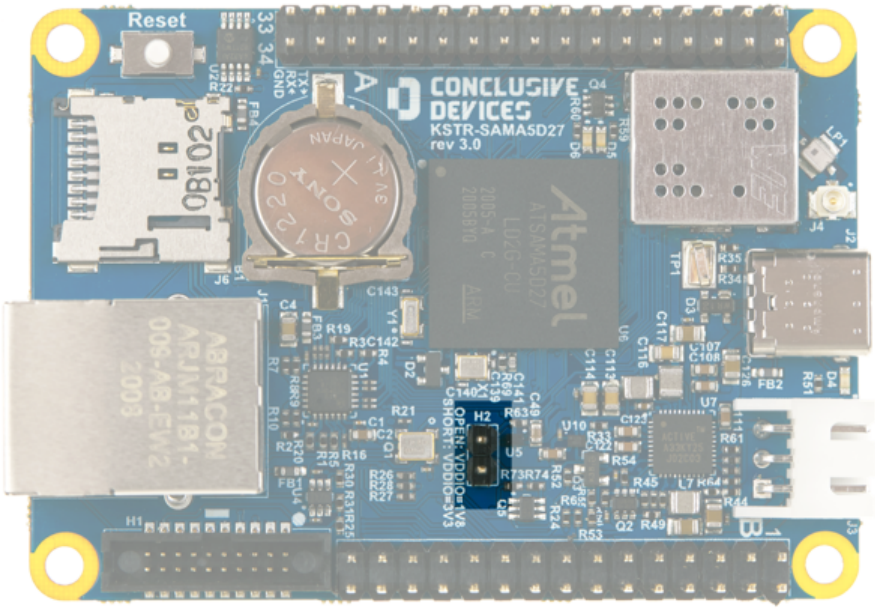


Fig. 6.9 VDDIO regulation pins location

Pair of pins that regulate the VDDIO voltage power supply of the board to the GPIO pins.

- Open: VDDIO power supply at 3.3V
- Short: VDDIO power supply at 1.8V

6.8. Status LEDs

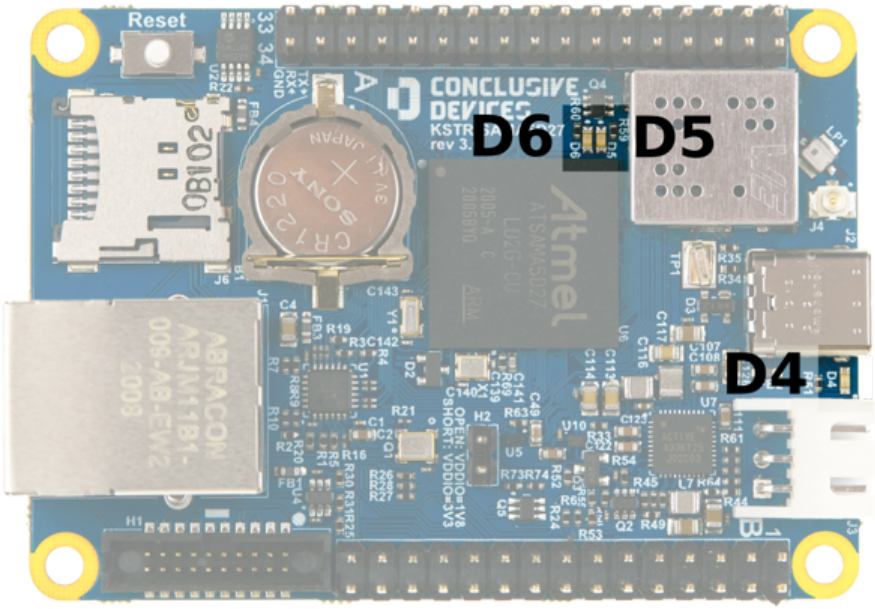


Fig. 6.10 Board status LEDs location

Three status LEDs.

- D4 - Not user-programmable. Power supply indicator LED. Turns on when power is supplied to the board via USB. Does not turn on when operating on battery.
- D5 - User-programmable. Default behavior is system load heartbeat indicator. Increases blinking frequency depending on board compute load as indicated by the installed operating system.
- D6 - User-programmable. Default behavior is SD/MMC activity. Blinking frequency mirrors IO access to SD/MMC storage.

6.9. I2C Devices

The following devices are connected to the main system I2C bus of KSTR-SAMA5D27:

Table 6.1 Onboard I2C devices

Name	I2C Address
ACT8945A PMIC	0x5B
24AA32A EEPROM	0x50

7. External Connectors

7.1. microSD Card Connector

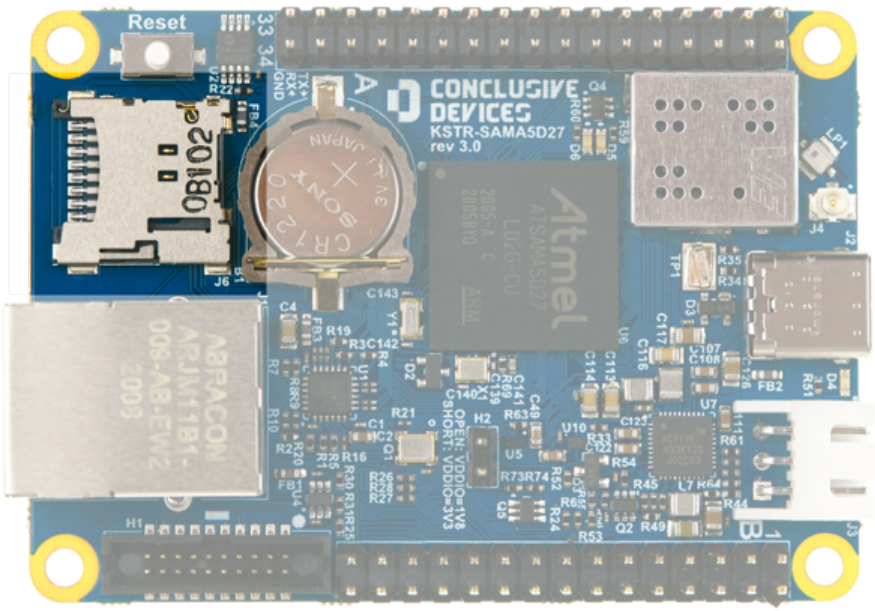


Fig. 7.1 SD card slot location

Supports SDSC, SDHC, SDXC, up to UHS-I SDR104

NOTE: Some SD cards implement the standard in uncommon ways. If you encounter a card that is unsupported by KSTR-SAMA5D27, please contact us so we can provide an update.

To enable SD card boot, KSTR-SAMA5D27 expects the first partition of the card to be formatted using FAT16 or FAT32 file systems. For more information please refer to the Boot process section.

7.2. CR1220 Coin Battery Holder

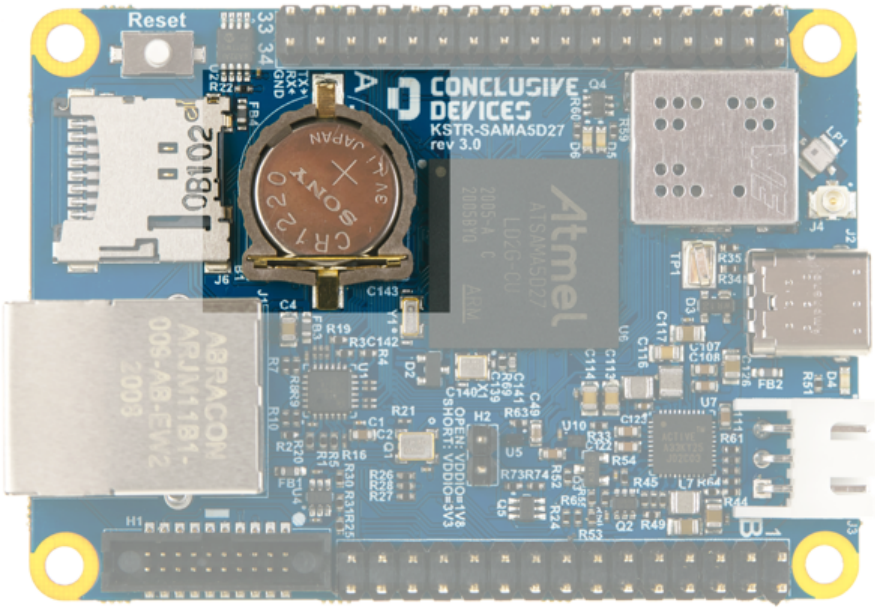


Fig. 7.2 CR1220 battery holder location

A single CR1220 Coin Battery holder. Battery delivers upkeep power for the RTC. It also upkeeps CPU internal backup registers that allow for boot selection bypassing the fuse bit. A compatible battery should be normally included with the board.

The battery provides power to the VDDBU power rail on ATSAMA4D27. It delivers power to:

- Slow Clock Oscillator
- Internal 64-kHz RC Oscillator
- part of the System Controller

For more information please refer to the ATSAMA5D27 technical documentation.

7.3. Wireless Antenna Coaxial Connector

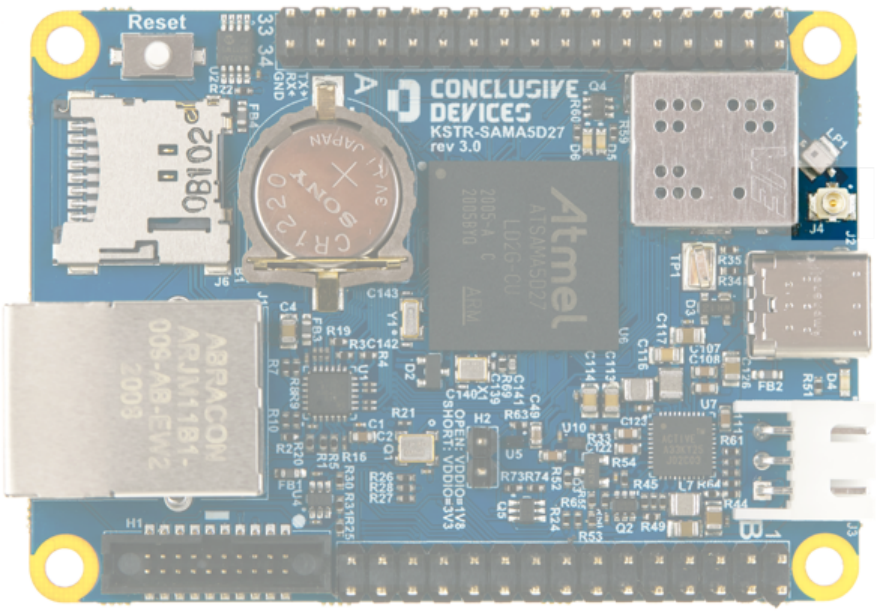


Fig. 7.3 Antenna coaxial connector location

A single connector for a wireless antenna. It's an ultra small surface mount coaxial connector, Hirose U.FL-R-SMT. Antenna is normally supplied with KSTR-SAMA5D27 in the Wireless-enabled variant.

7.4. Conclusive Developer Cable Connector

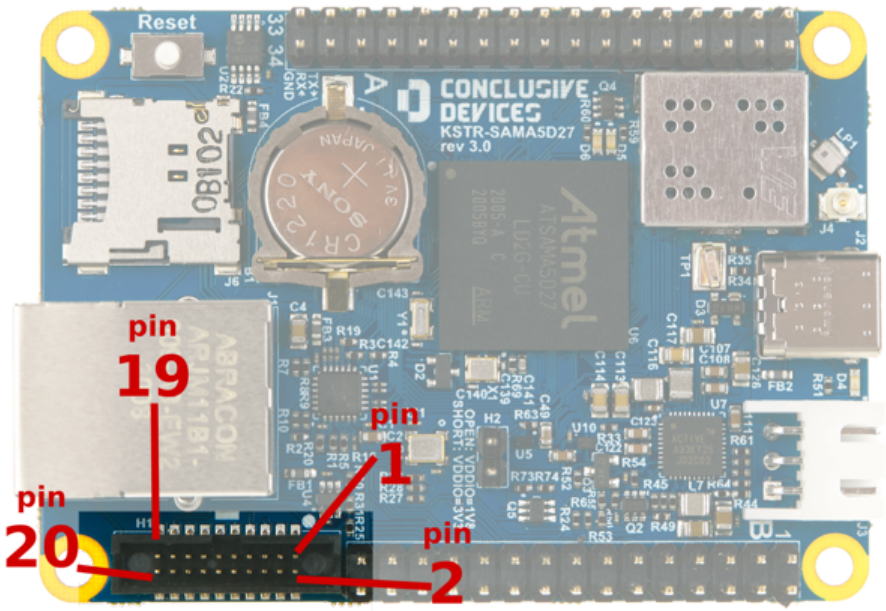


Fig. 7.4 Conclusive Developer Cable connector location

A 1.23mm 20-pin connector providing access to:

- Debug UART
- JTAG port
- System I2C bus

Pinout table continued on next page

Table 7.1 Developer Connector Pinout

Pin	Pin name	Direction	Description
1	VCC_IO	Power	Reference I/O voltage provided by the board
2	JTAG_TMS	In	JTAG test mode select
3	GND	Power	Ground
4	JTAG_TCK	In	JTAG clock
5	UART_RXD	Out	DEBUG_UART data receive signal
6	JTAG_TDO	Out	JTAG data output

Pin	Pin name	Direction	Description
7	UART_TXD	In	DEBUG_UART data transmit signal
8	JTAG_TDI	In	JTAG data input
9	JTAG_nTRST	In	JTAG test reset (active low)
10	JTAG_nRESET	In	JTAG reset (active low)
11	I2C_SCL	In/Out	SYS_I2C clock
12	JTAG_BSR_VSEL	In	An IEEE 1149.1 JTAG Compliance Enable
13	I2C_SDA	In/Out	SYS_I2C data
14	JTAG_TBSCAN_EN	In	An IEEE 1149.1 JTAG Compliance Enable
15	EEPROM_WP	In	EEPROM write protection (active low)
16	DEBUG_UART_MUX	In	Switch DEBUG_UART between Developer cable connector and Micro-B USB port
17	JTAG_HRESET_B	In	HRESET input (active low)
18	GND	Power	Ground
19	GND	Power	Ground
20	GND	Power	Ground

7.5. RJ45 10/100 Ethernet Connector

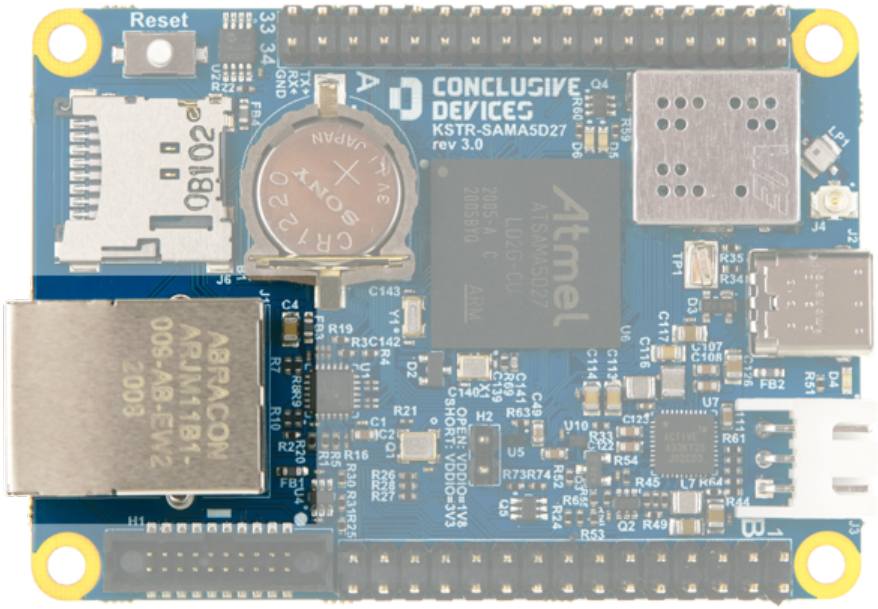


Fig. 7.5 RJ45 Ethernet port location

A single RJ45 10/100 Mbit Ethernet connector.

7.6. External Battery Connector

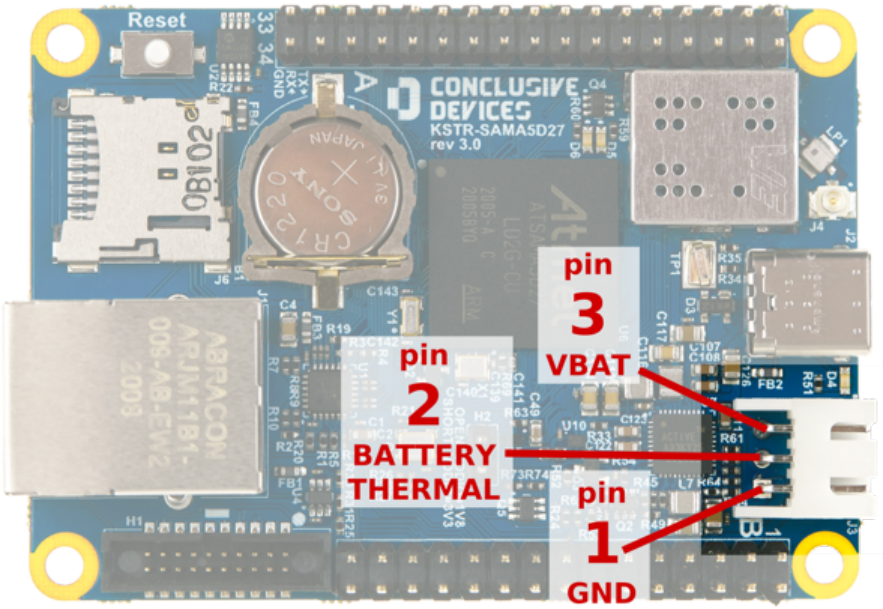


Fig. 7.6 External Battery Connector location

An S3B-XH-A 2.50mm pin pitch 3-pin connector for external battery power supply. Supports a single Li-Ion or Li-Poly battery. Provides charging and temperature monitoring. It's managed by the ACT8945A ActivePMU PMIC.

Table 7.2 External battery connector pinout

Pin	Description
1	Ground
2	Battery NTC resistor
3	Battery positive terminal

7.7. USB-C Connector

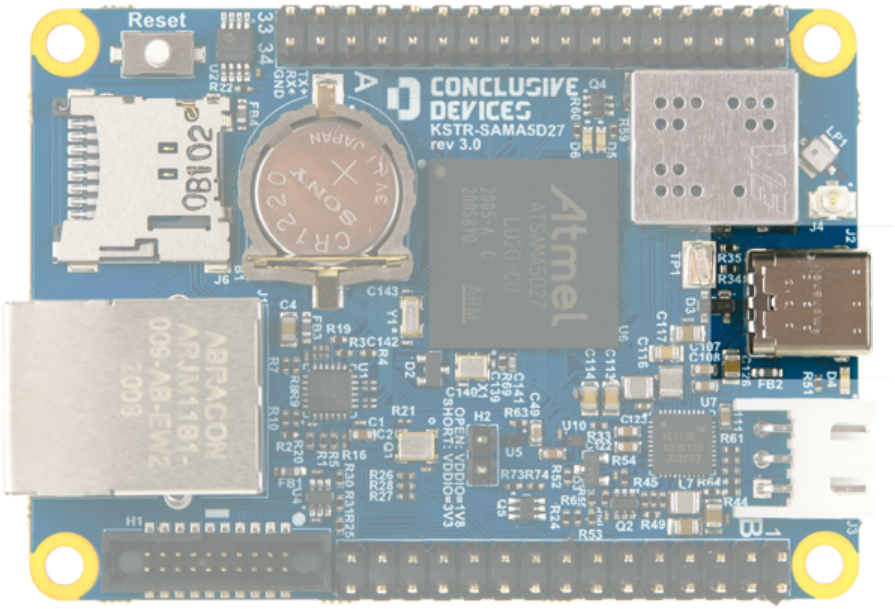


Fig. 7.7 USB-C Connector location

A single USB-C connector that allows connecting to KSTR-SAMA5D27 in device mode. Provides power to the board, some power supply pins on Headers A and B (see pinout reference), and battery charging function. If a charged battery is attached to the board, a breakage in USB-C power delivery will uninterruptibly switch to battery power.

7.8. I/O Expansion Headers Diagram

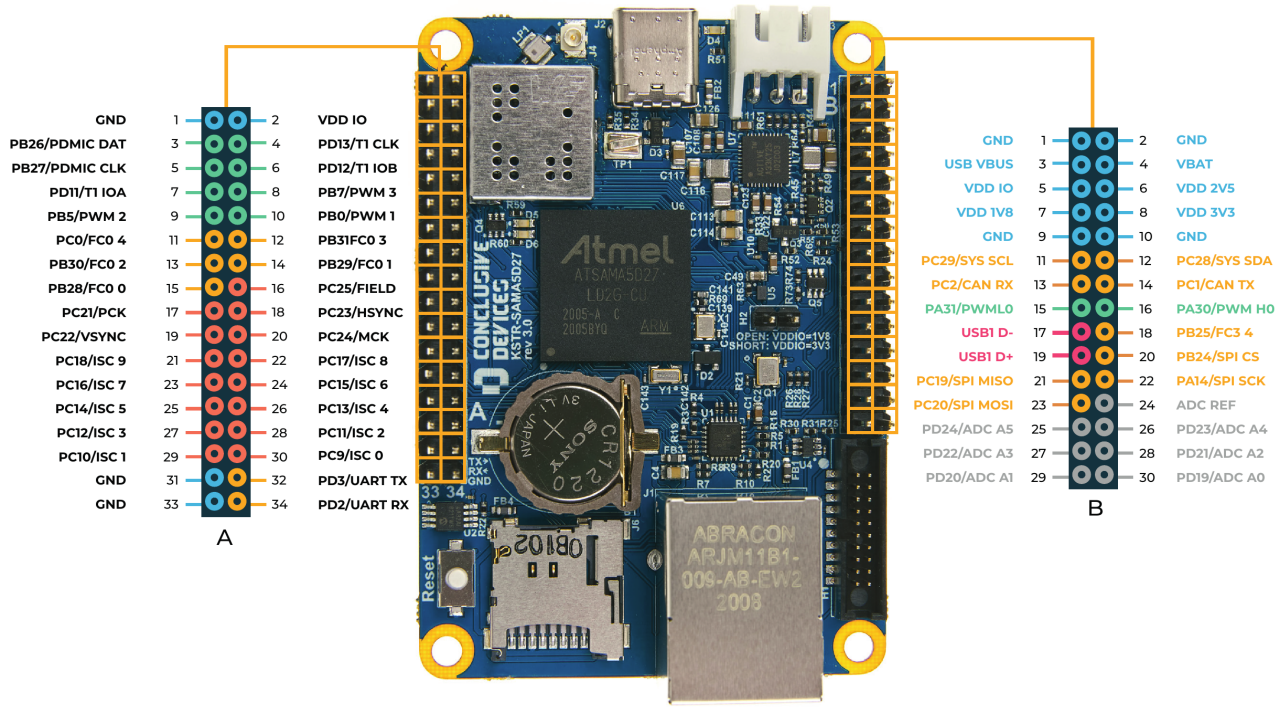


Fig. 7.8 Expansion Headers Pin Diagram

7.9. I/O Expansion Header A

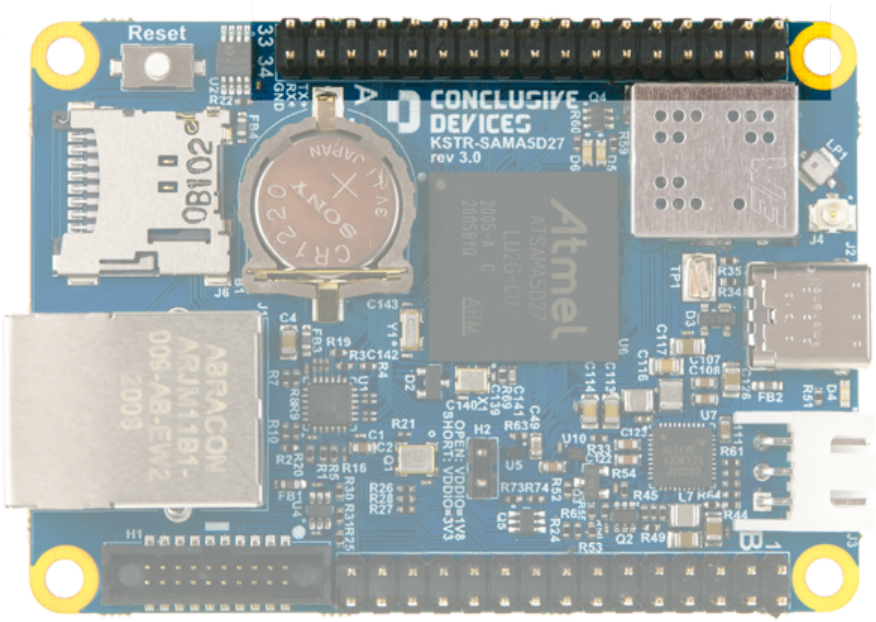


Fig. 7.9 Expansion Header A location

The tables below describe pin functions on the I/O expansion header A. Additionally the table provides references to the BGA ball map of ATSAMA5D27 when possible. KSTR-SAMA5D27 uses the 361 BGA socket variant of ATSAMA5D27

Table 7.3 I/O Expansion Header A pinout

Pin	Pin Name	Pin Function	SoC Pin
1	GND	Ground	
2	VDD_IO	IO Voltage	
3	H1_PDMIC_DAT	Pulse Density Modulation (PDMIC) Data	G2
4	H1_T1_CLK	Timer External Clock Input	N2
5	H1_PDMIC_CLK	Pulse Density Modulation (PDMIC) Clock	H5
6	H1_T1_IOB	Timer I/O Channel B	M7
7	H1_T1_IOA	Timer I/O Channel A	N3
8	H1_PWM3	PWM Channel 3	C5
9	H1_PWM2	PWM Channel 2	A7

Pin	Pin Name	Pin Function	SoC Pin
10	H1_PWM1	PWM Channel 1	C7
11	H1_FC0_4	FLEXCOM 0 I/O 4	T14
12	H1_FC0_3	FLEXCOM 0 I/O 3	J4
13	H1_FC0_2	FLEXCOM 0 I/O 2	A2
14	H1_FC0_1	FLEXCOM 0 I/O 1	J3
15	H1_FC0_0	FLEXCOM 0 I/O 0	J2
16	H1_FIELD	Field Identification Signal (ISC)	L4
17	H1_PCK	Image Sensor Pixel Clock (ISC)	E3
18	H1_HSYNC	Image Sensor Horizontal Sync (ISC)	L7
19	H1_VSYNC	Image Sensor Vertical Sync (ISC)	E2
20	H1_MCK	Image Sensor Main Clock (ISC)	E1
21	H1_ISC_9	Image Sensor Data 9 (ISC)	L9
22	H1_ISC_8	Image Sensor Data 8 (ISC)	C1
23	H1_ISC_7	Image Sensor Data 7 (ISC)	K9
24	H1_ISC_6	Image Sensor Data 6 (ISC)	B1
25	H1_ISC_5	Image Sensor Data 5 (ISC)	K6
26	H1_ISC_4	Image Sensor Data 4 (ISC)	K2
27	H1_ISC_3	Image Sensor Data 3 (ISC)	D2
28	H1_ISC_2	Image Sensor Data 2 (ISC)	C2
29	H1_ISC_1	Image Sensor Data 1 (ISC)	K5
30	H1_ISC_0	Image Sensor Data 0 (ISC)	B2
31	GND	Ground	
32	UART_TX	Debug UART Transmit	M3

Pin	Pin Name	Pin Function	SoC Pin
33	GND	Ground	
34	UART_RX	Debug UART Receive	J6

7.10. I/O Expansion Header B

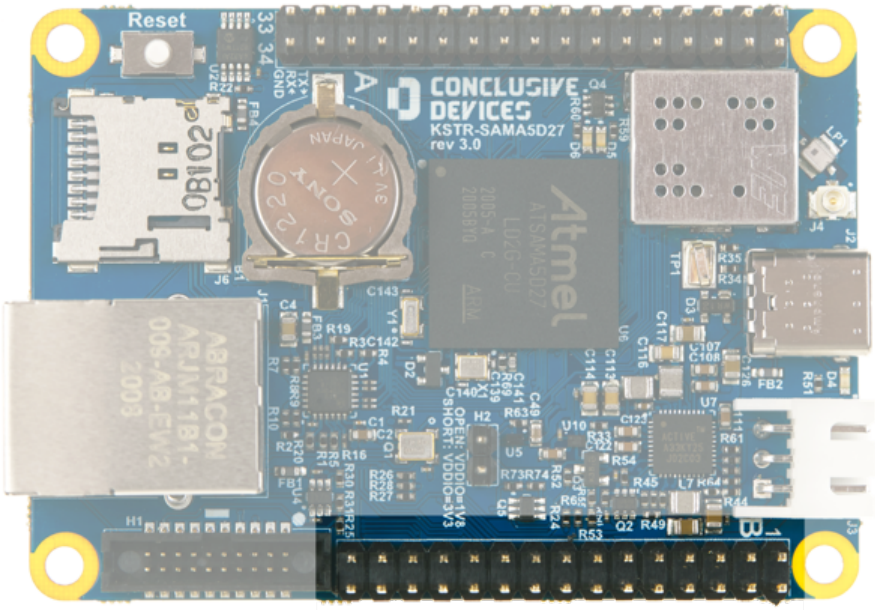


Fig. 7.10 Expansion Header B location

The tables below describe pin functions on the I/O expansion header B. Additionally the table provides references to the BGA ball map of ATSAMA5D27 when possible. KSTR-SAMA5D27 uses the 361 BGA socket variant of ATSAMA5D27

Table 7.4 I/O Expansion Header B pinout

Pin	Pin Name	Pin Function	SoC Pin
1	GND	Ground	
2	GND	Ground	
3	USB_VBUS	USB Power (forwarded from USB-C) (5V)	
4	VBAT	Li-Ion/Li-Poly Battery Power Output	
5	VDD_IO	I/O Power Output	
6	VDD_2V5	2.5V Power Output	
7	VDD_1V8	1.8V Power Output	
8	VDD_3V3	3.3V Power Output	
9	GND	Ground	

Pin	Pin Name	Pin Function	SoC Pin
10	GND	Ground	
11	SYS_SCL	System I2C Clock	C6
12	SYS_SDA	System I2C Data	J5
13	H2_CAN_RX	CAN Receive	T15
14	H2_CAN_TX	CAN Transmit	R16
15	H2_PWM_L0	Differential PWM Output Low	U17
16	H2_PWM_H0	Differential PWM Output High	U12
17	USB1_D_N	USB1 DM (Data Minus)	V8
18	H2_FC3_4	FLEXCOM 3 I/O 4	H1
19	USB1_D_P	USB1 DP (Data Plus)	W8
20	H2_FC3_3	FLEXCOM 3 I/O 3	A3
21	H2_FC3_1	FLEXCOM 3 I/O 1	D1
22	H2_FC3_2	FLEXCOM 3 I/O 2	R19
23	H2_FC3_0	FLEXCOM 3 I/O 0	L8
24	H2_ADCREF	ADC Reference Voltage Input	M9
25	H2_ADC_A5	ADC Channel 5	N8
26	H2_ADC_A4	ADC Channel 4	P1
27	H2_ADC_A3	ADC Channel 3	N6
28	H2_ADC_A2	ADC Channel 2	P3
29	H2_ADC_A1	ADC Channel 1	N1
30	H2_ADC_A0	ADC Channel 0	M8

8. Electrical Specification

8.1. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings

Pin	Min	Max	Units	Comments
VBAT	-0.5	6.0	V	Li-Ion/Li-Poly battery power rail
VBUS	-0.3	6.0	V	USB Power
USB pins	-0.5	6.0	V	
GPIO	-0.5	4.0	V	Maximum DC input VIN voltage on GPIO

8.2. Recommended Operating Conditions

Table 8.2 Recommended operating conditions

Pin	Min	Typ	Max	Units	Comments
VBAT	3.0	3.7	4.2	V	Li-Ion/Li-Poly battery power rail
VBUS	0.0	5.0	5.5	V	USB Power
USB pins	0.0		3.6	V	
GPIO	0.0		VDD_IO	V	Maximum DC input VIN voltage on GPIO

8.3. Output Power Supplies

KSTR-SAMA5D27 exposes six general purpose switching power supplies. Maximum user current draw from each rail is described in the table below:

Table 8.3 Output power supplies

Voltage, V	Available current, mA	Location (header)	Comment
1.8	500	HB_7	
2.5	300	HB_6	
3.3	500	HB_8	
3.7	2000	HB_4	Limited by I/O header and battery capabilities.
5.0	2000	HB_3	Limited by USB power source capabilities.
1.8/3.3 (I/O)	500	HA_2, HB_5	Power limit of the I/O rail is the power limit of the respective power rail (1.8/3.3V).

Note: Total current draw from all PMIC provided power rails combined (1.8V, 2.5V, 3.3V) must not exceed 1.0A. Exceeding this value will result in damage to the board.

9. Environmental Specifications

Table 9.1 Environmental specification

Parameter	Min	Max
SoC Operating temperature range	-40° C	+85° C
Storage Temperature	-60° C	+150° C
SoC Junction temperature	-40° C	+125° C

WARNING: System with an installed CR1220 battery must not exceed the temperature range of 0° C to +30° C at any time due to battery temperature limits. After installing a Li-Ion or Li-Poly battery, please respect their temperature limits.

To exceed this limit, please remove or change the CR1220 battery to one certified for target temperature use

10. SBC Dimensions

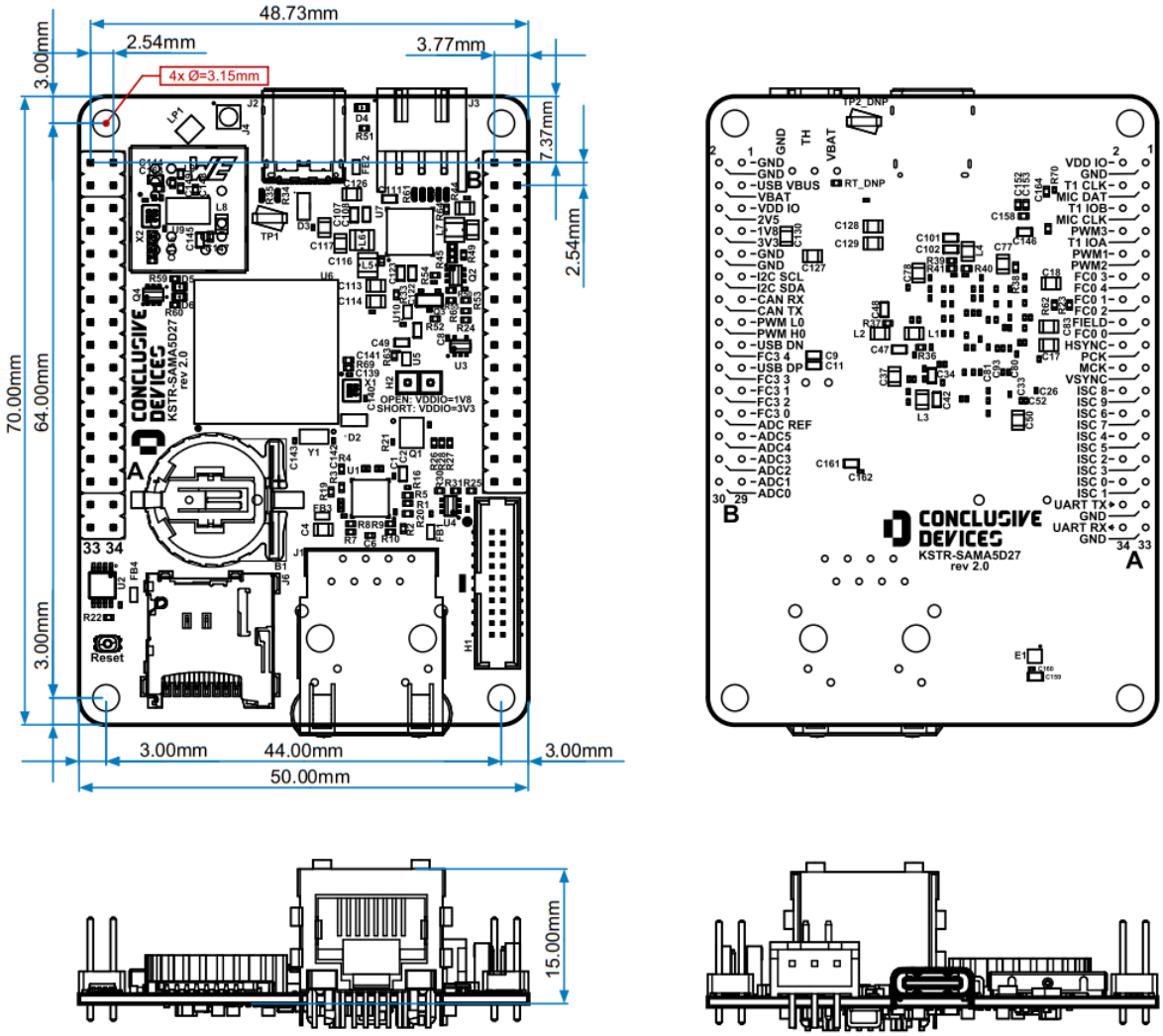


Fig. 10.1 KSTR-SAMA5D27 Top View Mechanics in millimeters

11. Boot process

This section summarizes boot options for KSTR-SAMA5D27.

11.1. ROM Boot

KSTR-SAMA5D27 1st stage bootloader is embedded in ROM memory of the Microchip ATSAMA5D27 processor. Boot methods and boot media order can be set via Boot Word configuration is SRAM, or via fuse bits, depending on the microprocessor's configuration. Please refer to ATSAMA5D27 documentation for details, or contact us directly regarding custom boot implementations. In its default state, KSTR-SAMA5D27 is booting from the microSD card, placed in its microSD card connector, available to the microprocessor via the SDMMC0 interface. It expects to find next stage bootloaders and root filesystem on an inserted SD card.

11.2. AT91Bootstrap

Second stage bootloader is an AT91Bootstrap configured for the KSTR-SAMA5D27 board. The role of this bootloader is very similar to the SPL part of U-Boot. KSTR-SAMA5D27 expects that:

- The SD card's first partition is formatted with either FAT16 or FAT32 file system.
- Binary form of the bootloader is placed on the root of this partition, and named *boot.bin*.

Currently KSTR-SAMA5D27 is supporting AT91Bootstrap version 3.10.0

11.3. U-Boot

Das U-Boot is the 3rd stage bootloader. It loads the Linux kernel directly. In its default configuration, KSTR-SAMA5D27 expects a file named *u-boot.bin* on the root of the first SD card partition, the same as the above AT91Bootstrap binary. Additional environment configuration settings for U-Boot can be delivered by stored in a file named *uboot.env* placed on the SD card's first partition root directory. Currently KSTR-SAMA5D27 supports U-Boot version 2021.04, but this is regularly kept up to date with board startup package releases.

11.4. Linux

Currently KSTR-SAMA5D27 supports Linux kernel version 5.10. Conclusive Engineering provides support for newer kernels continuously, as part of the board startup package updates, so usually kernel version support should be up to date or become available shortly after a new kernel release. We can provide support for older kernels to match specific client's needs.

12. Ordering information

KSTR-SAMA5D27 is currently available in one variant. It can be ordered directly on our website: https://store.conclusive.pl

To obtain the KSTR-SAMA5D27 variant without the WiFi module, please contact us directly.

Build date: 2022-05-13 21:23:01. Release version: b43de49.
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